CHAPTER 5. CIRCUIT DESCRIPTION

[1] Circuit description

1. General description

In this machine, the facsimile control block except the printer control is mainly composed of the units shown in Fig. 1.

2. PWB configuration

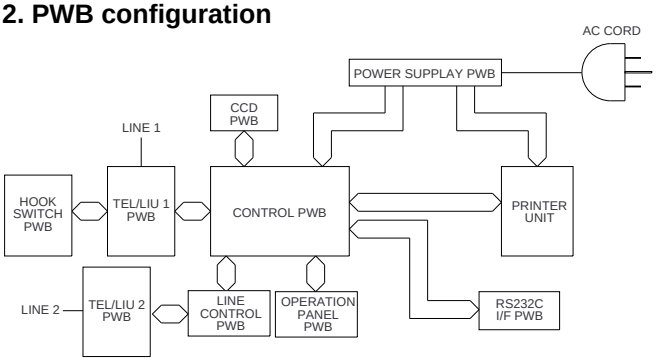


Fig. 1

1) Control PWB

The control PWB controls all the other operations except the printing operation of the printer and the 2nd line control.

2) Line control PWB

The line control PWB controls TX/RX of 2nd line.

3) TEL/LIU 1, 2 PWB

The TEL/LIU PWB controls the I/F telephone function of the circuit with the control signals from the control PWB or the line control PWB.

4) CCD PWB

CCD PWB converts the image of the sending or copying draft into the photoelectric signals and transmits the signals to the control PWB.

5) Operation panel PWB

The operation panel PWB detects the key input, turns on and off LED and displays LCD according to the control signals from the control PWB.

6) Power supply PWB

DC voltages (+5V, +12V, +24V) are produced from AC120V, and are supplied to the printer unit and control PWB unit.

7) RS232C I/F PWB

The voltage level of the interface signals to PC is converted.

[2] Circuit description of control PWB

1. General description

The control PWB is composed of the following blocks.

① Main control block
② EPROM, DRAM, RTC block
③ Image memory block
④ Modem-1 block
⑤ Reading process and mechanical control block
⑥ Gate array (A) block
⑦ Gate array (B) block
⑧ CODEC block
⑨ Page memory block
⑩ Driver block
⑪ Connector block (CNSB)
⑫ Access control block
⑬ Sub-1 CPU block
⑭ Sub-1 ROM, DRAM block
⑮ Dual port RAM-1 block
⑯ Connector block (CNLIU)
⑰ Sub-1 access control block

2. Description of each block

(1) Main control block

The main control block uses RISC microprocessor HD6437021 as CPU, being composed of ROM (1 MByte) and DRAM (512 KByte).

1) HD6437021 (IC13): pin-100, QFP (main CPU)

The device is a microprocessor which integrates the peripheral functions, using CPU of 32-bit RISC type as the core. In the instrument, the following peripheral functions are mainly used.

① ROM of 32 KByte and RAM of 1 KByte are integrated.
A part of programs are stored in the integrated ROM.

② DMA controller (4 channels are provided, and 2 channels alone are used.)
ch.0: Used to transmit image data between CODEC (HM514260) and DRAM(IC7).
ch.3: Used to transmit image data between CPU and DRAM(IC7).

③ Clock-synchronous type serial communication interface Commands and statuses are communicated with PCU.

④ Start-stop synchronous type serial communication interface Used for PC interface of RS232C system.

⑤ Interruption
$\overline{IRQ2}$: Interruption request from gate array (A) (LZ9FJ37A)
$\overline{IRQ3}$: Interruption request from gate array (B) (LR38292)
$\overline{IRQ4}$: Interruption request from CODEC (HD813201F)
$\overline{IRQ6}$: Interruption request from dual port RAM of sub-2 (IDT7130/ IDT7140)
$\overline{IRQ7}$: Interruption request from dual port RAM of sub-1 (IDT7130/ IDT7140)
$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ5}$: Not used.
$\overline{NMI}$: Not used.

⑥ DRAM controller
Addressing to DRAM(IC7) of the system and control and refresh control of $\overline{RAS}$ and $\overline{CAS}$ signals are executed.

⑦ Timer and watch dog timer

⑧ General-purpose I/O port
Control of analog process of read signals are executed.

⑨ Clock oscillation
Ceramic oscillator of 19.66 MHz is connected for operation of 19.66 MHz.

(2) EPROM, DRAM, RTC block

1) 27C040 (IC5, 11): pin-32, DIP (ROM)

Programs are stored in two 4 Mbit ROM.

2) HM514260 (IC7): pin-40, SOJ (DRAM)

Used as the system memory of main CPU and transmission buffer of communication.

3) NJU6355E (IC127): pin-8, SOP (Real time clock IC)

It is oscillated with the quartz oscillator of 32.768 kHz, and the clock and calendar functions are provided. Even if the power supply of the main body is turned off, it is backed up with lithium battery. This device executes the clock-synchronous type serial communication with the gate array (A), and CPU can know the time and date through the gate array (A).

HD6437021 (IC13) Terminal descriptions

Classification	Code	Terminal No. (TFP-100B)	I/O	Name	Function
Power	Vcc	13, 38, 63, 73, 80, 88	I	Power	Connect to the power supply. Connect Vcc terminals to the power units of all systems. If any open terminal is present, it will not operate
	Vss	4,15,24,32, 41,50,59,70, 81,82, 92	I	Ground	Connect to the ground. Connect Vcc terminals to the power units of all systems. If any open terminal is present, it will not operate.
Clock	EXTAL	71	I	External clock	Connect to the quartz oscillator. Moreover, EXTAL terminal can input the external clock. Use the same frequency for the quartz oscillator, external clock and system clock.
	XTAL	72	I	Crystal	Connect the quartz oscillator. Connect the same frequency of the system clock (CK). To input external clock from EXTAL terminal, open EXTAL terminal.
	CK	69	O	System clock	Supply system clock to the peripheral device.
System control	$\overline{\text{RES}}$	76	I	Reset	If this terminal is turned to the low level when NMI is at the high level, it will be brought into the power-on state. If this terminal is turned to the low level when NMI is at the low level, it will be brought into the manual.reset state.
	$\overline{\text{WDTOVF}}$	75	O	Watch dog timer overflow	It is overflow output signal from WDT.
	$\overline{\text{BREQ}}$	60	I	Bus right request	Select the low level to make the external device request the release of bus right.
	$\overline{\text{BACK}}$	58	O	Bus right request acknowledge	It indicates that the bus right is released to the external device. When receiving $\overline{\text{BACK}}$ signal, the device which outputs $\overline{\text{BREQ}}$ signal can know that bus right is obtained.
Operation mode control	MD2~ MD0	79~77	I	Mode setting	The terminal determines the operation mode. During operation, don't vary any input value. The relationship between MD2 thru MD0 and operation modes are shown in the following list.
Interrupt	NMI	74	I	No-maskable interrupt	This is the interrupt request terminal which can not be masked. Either leading edge or trailing edge is selected for receiving.
	$\overline{\text{IRQ0}}$~ $\overline{\text{IRQ7}}$	65,66,67,68, 97,98,99,100	I	Interrupt request 0 thru 7	This is the interrupt request terminal which can be masked. Either level input or edge input can be selected.
	$\overline{\text{IRQOUT}}$	61	O	Interrupt request output in the slave mode	It indicates that a factor of interrupt occurs. It indicates that interrupt occurs in the bus release mode.
Address	A21~A0	45~42,40,39, 37~33,31~25, 23~20	O	Address	Address is output.
Data bus	AD15~ AD0	19~16,14, 12~5,3~1	I/O	Data bus	Bidirectional data bus of 16 bits Multiplex is possible with the low-order 16 bits of the address.
	DPH	64	I/O	High-order side data bus parity	Parity data corresponds to D15 thru D8.
	DPL	62	I/O	Low-order side data bus parity	Parity data corresponds to D7 thru D0.

(Continuing)

Relationship between MD2 thru MD0 and operation modes

MD2	MD1	MD0	Operation mode	IntegratedROM	Bus width of area 0
0	0	0	MCU mode	Invalid	8-bit size
0	0	1			16-bit size
0	1	0		Valid	—
0	1	1	(Reserved)	—	—
1	0	0	(Reserved)	—	—
1	0	1	(Reserved)	—	—
1	1	0	(Reserved)	—	—
1	1	1	(Reserved)	—	—

HD6437021 (IC13) Terminal descriptions

Classification	Code	Terminal No. (TFP-100B)	I/O	Name	Function
Bus control	$\overline{WAIT}$	54	I	Wait	It is input to insert Tw into the bus cycle during access to the external space.
	$\overline{RAS}$	52	O	Low address strobe	Timing signal of low address strobe of DRAM
	$\overline{CASH}$	47	O	High-order column address strobe	Timing signal of column address strobe of DRAM It is output for access to high-order 8 bits of data.
	$\overline{CASL}$	49	O	Low-order column address strobe	Timing signal of column address strobe of DRAM It is output for access to low-order 8 bits of data.
	$\overline{RD}$	57	O	Read	It indicates that outside is read out.
	$\overline{WRH}$	56	O	High-order write	It indicates writing at the external high-order 8 bits.
	$\overline{WRL}$	55	O	Low-order write	It indicates writing at the external low-order 8 bits.
	$\overline{CS0}$~$\overline{CS7}$	46~49, 51~54	O	Chip select 0 thru 7	Chip select signal for external memory or device
	$\overline{AH}$	61	O	Address hold	Address hold timing signal for device which uses multiplex bus of address/data
	$\overline{HBS}$, $\overline{LBS}$	20 56	O	Low-/high-order byte strobe	Strobe signal of high/low byte (Commonly used with AO, $\overline{WRH}$.)
	$\overline{WR}$	55	O	Write	Output during writing. (Commonly used with $\overline{WRL}$.)
DMAC	$\overline{DREQ0}$, $\overline{DREQ1}$	66,68	I	DMA transfer request (Channels 0 and 1)	Input terminal of DMA transfer request from external
	DACK0, DACK1	65,67	O	DMA transfer request receiving (Channels 0 and 1)	It indicates that DMA transfer request is received.
16-bit integrated timer pulse unit (ITU)	TIOCA0, TIOCB0	51, 53	I/O	ITU input capture/output conveyor (Channel 0)	Output terminal of input capture input/output conveyor
	TIOCA1, TIOCB1	62, 64	I/O	ITU input capture/output conveyor (Channel 1)	Output terminal of input capture input/output conveyor
	TIOCA2, TIOCB2	83, 84	I/O	ITU input capture/output conveyor (Channel 2)	Output terminal of input capture input/output conveyor
	TIOCA3, TIOCB3	85, 86	I/O	ITU input capture/output conveyor (Channel 3)	Output terminal of input capture input/output conveyor
	TIOCA4, TIOCB4	87, 89	I/O	ITU input capture/output conveyor (Channel 4)	Output terminal of input capture input/output conveyor
	TOCXA4, TOCXB4	90, 91	O	ITU output conveyor (Channel 4)	Output terminal of output conveyor
	TCLKA~ TCLKD	65,66,90, 91	I	ITU timer clock input	External clock input terminal to counter of ITU
Timing pattern controller (TPC)	TP15~ TP0	100~93, 91~89, 87~83	O	Timing pattern Output 15 thru 0	Output terminal of timing pattern
Serial communication nterface (SCI)	TxD0, TxD1	94, 96	O	Sending data (Channels 0 and 1	Sending data output terminal of SCI0, 1
	RxD0, RxD1	93, 95	I	Receiving data (Channels 0 and 1)	Receiving data input terminal of SCI0, 1
	SCK0, SCK1	97, 98	I/O	Serial clock (Channels 0 and 1)	Clock input/output terminal of SCI0, 1
I/O port	PA15~ PA0	68~64, 62~60, 58~51	I/O	Port A	Input/output terminal of 16 bits Input/output can be assigned for each bit.
	PB15~ PB0	100~93, 91~89, 87~83	I/O	Port B	Input/output terminal of 16 bits Input/output can be assigned for each bit.

(3) Image memory block

This block is composed of 2 MByte flash memory and 128 KByte SRAM. Moreover, a maximum of 16 MByte (when FO-16MG is installed) of image memory can be extended by install-ing the option memory of the connector CNOP.

1) LH28F016SUT (IC6) — Pin-56, TSOP (16 Mbit flash memory)

The memory is a non-volatile type whose content does not erase even if power is turned off, and stores the copied, sent and received image data. Moreover, the initially registered data, registered content of "RELAY" key and registered content of "CONF" key are stored.

2) KM68512ALG-5L(IC2, IC9) — pin-32, SOP (512 Kbit SRAM)

The setting of receiving mode, optional setting content, soft switch content and dairy data are stored. Even if the power supply of the main body is turned off, it is backed up with a lithium battery.

The above functions are controlled by getting an access to the inter-face memory in the modem through the data bus from sub-1 CPU (IC4) of the control PWB. The interface memory is composed of 32 8-bit registers, and is controlled with the bank switch. Accordingly, the register is selected by the register selection signals (RS4 to RS0) of 5 bits and chip selection signal (CS). The major content controlled by these reg-isters is as follows.

1) Configuration register

Mode setting of V34, V17, V29, V27, G2, FSK and tone transmission

2) Option register

Equalizing method of equalizer, carrier detection threshold, addition of echo suppressor protect tone, and setting of transmission/reception mode

3) Others

G2AGC control, tone frequency setting, and so on

Moreover, data is read from these registers through the data bus to monitor the statuses of the modem such as tone detection, training pattern detection and so on.

Next, transmission/reception operation is described.

During sending, the sent data is given from the control block to the modem through the data bus. Then, it is modulated and sent to TEL/LIU 1 PWB with SIGTX signal. During receiving, the received data is sent from TEL/LIU 1 PWB to the modem with SIGRX signal and is demodulated. Then, it is sent to the control block with the data bus. The above operation is done with the modem LSI (IC).

(4) Modem-1 block

The block is mainly composed of the modem R288F (IC3), and is provided with the following modem function.

Configuration	Modulation 1	Carrier Frequency (Hz) ± 0.01 %	Data Rate (bps) ± 0.01 %	Symbol Rate (Symbols/Sec.)	Bits/Symbol-Data	Bits/Symbol-TCM	Constellation Points
V. 34 33600 TCM	TCM	Note 2	33600	3429 only	Note 2	Note 2	Note 2
V. 34 31200 TCM	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V. 34 28800 TCM	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V. 34 26400 TCM	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V. 34 24000 TCM	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V. 34 21600 TCM	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V. 34 19200 TCM	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V. 34 16800 TCM	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V. 34 14400 TCM	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V. 34 12000 TCM	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V. 34 9600 TCM	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V. 34 7200 TCM	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V. 34 4800 TCM	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V. 34 2400 TCM	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V. 23 1200/75	FSK	1700/420	1200/75	1200	1	0	—
V. 21	FSK	1080/1750	0-300	300	1	0	—
V. 17 14400 TCM	TCM	1800	14400	2400	6	1	128
V. 17 12000 TCM	TCM	1800	12000	2400	5	1	64
V. 17 9600 TCM	TCM	1800	9600	2400	4	1	32
V. 17 7200 TCM	TCM	1800	7200	2400	3	1	16
V. 29 9600	QAM	1700	9600	2400	4	0	16
V. 29 7200	QAM	1700	7200	2400	3	0	8
V. 29 4800	QAM	1700	4800	2400	2	0	4
V. 27 4800	DPSK	1800	4800	1600	3	0	8
V. 27 2400	DPSK	1800	2400	1200	2	0	4
V. 21 Channel 2	FSK	1750	300	300	1	0	—

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation QAM: Quadrature Amplitude Modulation
   FSK: Frequency Shift Keying DPSK: Differential Phase Shift Keying
2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	V. 34 Low Carrier	V. 34 High Carrier
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

(5) Reading process and mechanical control block

1) Reading process block

The reading block is composed of the following blocks.

① CCD drive block (IC14: LZ9FJ37A)

② Analog process block
- Analog LSI(IC25: TLS1049)
- Tr.C/R etc

③ Binary coding block/read data control block (IC14:LZ9FJ37A)

The details of each block are described as follows.

a) CCD drive block

The clock signal necessary for CCD drive is supplied from gate array (A) to CCD.
Hereafter, the clocks are outlined.
- ϕT -- Line synchronous signal
- ϕ1/ϕ2 --- Transmission clock

b) Analog process block

The analog video signal supplied from CCD PWB is directly supplied to the analog LSI.

On the other hand, as the reference level (reference voltage) of A/D conversion, the peak voltage of the video signal detected in the peak hold circuit is supplied to the A/D conversion block in the stan-dard/ fine/ super fine mode and the fixed voltage is supplied to the block in the half tone mode. After the offset part is cut in the analog LSI, 7-bit digital video signal is supplied to the gate array by using the integrated 7-bit high speed A/D converter according to the A/D con-version clock output from the gate array.

c) Binary coding block/read data control block

It is composed of the processing circuit (IC14: LZ9FJ37A) which integrates various binary coding algorithms and the reading line memo-ries (IC23, IC24: LH5268TH10) which record necessary data. The digital video signal input in 7 bits is judged as 2 values (black(1) and white (0), and the data is transmitted to the gate array (B) (IC18: LR38292) in the serial mode and is stored in the page memory. The contents binary-coded here are as follows.
- Shading compensation
- Half tone process (error diffusion process)
- MTF compensation

2) Mechanical control block

The mechanical control block is mainly composed of the gate array (A) (IC14: LZ9FJ37A) to control the following.

(a) Sending motor control

The revolution speed and timing of the sending motor are controlled to output the control signals to the motor driver (IC20, IC21).

(b) End stamp and LED lamp control

On/off of the end stamp and LED lamp is controlled with the software.

(6) Gate array (A) block

This block is mainly composed of the gate array (A) (IC14: LZ9FJ37A), and has the following functions.

① Mapper
Mapping is executed in the memory area of the memories, gate array (B), modem and CODEC.

② Reading process
Refer to 1) Reading process block of 2-4 Reading and mechanical control block.

③ Mechanical control block
Refer to 2) Mechanical control block of 2-5 Reading and mechani-cal control block.

④ IC interface for clock
Writing and reading to IC (IC127: NJU6355E) for clock is executed in the clock-synchronous type serial transfer mode.

⑤ PC interface
- I/O port control (communication is done with main CPU.)
- Detection of communication speed with AT command monitor

⑥ Generation of alarm sound and ringer sound
The keys on the operation panel are pressed to respectively generate the key input sound, alarm sound and ringer sound.

LZ9FJ37A (IC14) Terminal descriptions

PIN	I/O	Name	Function	PIN	I/O	Name	Function
1	O	DP	Dial pulse control	52	I/O	D14	System data input/output
2	O	DT4	Output port	53	I/O	D13	System data input/output
3	O	DT3	Output port	54	I/O	D12	System data input/output
4	O	DT2	Output port	55	I	XCS6	Chip select 6 signal input
5	O	DT1	Output port	56	I	XCS2	Chip select 2 signal input
6	O	BZ	Buzzer output	57	I/O	D11	System data input/output
7	O	BZSL	Output port	58	I/O	D10	System data input/output
8	I	SDT	Input port	59	I/O	D9	System data input/output
9	I	XRHS	Input port	60	I/O	D8	System data input/output
10	I	XCI	Input port	61	—	GND	Ground
11	I	XHS1	Input port	62	—	VDD	Power supply
12	I	XHS2	Input port	63	I/O	D7	System data input/output
13	I	XEXHS1	Input port	64	I/O	D6	System data input/output
14	I	XEXHS2	Input port	65	I/O	D5	System data input/output
15	O	CRNT	Output port	66	I/O	D4	System data input/output
16	O	TXB1	B-phase current control output 1	67	I	A19	System address input/output
17	O	TXB0	B-phase current control output 0	68	I	A20	System address input/output
18	O	TXA1	A-phase current control output 1	69	I	A21	System address input/output
19	O	TXA0	A-phase current control output 0	70	I/O	D3	System data input/output
20	—	VDD	Power supply	71	I/O	D2	System data input/output
21	—	GND	Ground	72	I/O	D1	System data input/output
22	O	TXPB	B-phase current direction setting	73	I/O	D0	System data input/output
23	O	TXPA	A-current direction setting	74	I	A6	System address input/output
24	O	LEDON	LED light source control	75	I	A5	System address input/output
25	O	PLG1ON	Plunger 1 control	76	I	A4	System address input/output
26	O	PLG0ON	Plunger 0 control	77	I	A3	System address input/output
27	—	GND	Ground	78	I	A2	System address input/output
28	I	CLKR	Sending system control basic clock input	79	I	A1	System address input/output
29	I	XFLBSY	Flash memory busy signal input	80	—	GND	Ground
30	O	FLBK1	Bank control 1	81	I	TEST	Test terminal
31	O	FLBK2	Bank control 2	82	O	XSCCLK	Reading serial clock
32	O	FLBK3	Bank control 3	83	O	XSRVID	Reading serial data
33	O	XFLOPT	Chip select (flash option)	84	O	XSTVD	Reading valid data output gate
34	O	XFLSTD	Chip select (flash standard)	85	I	TXIN	Data receiving from SH1
35	O	XPGMSL	Chip select (EPROM)	86	O	RXOUT	Data sending to SH1
36	O	XSRAM1	Chip select (SRAM option)	87	O	TXOUT	Data sending signal to PC
37	O	XSRAM0	Chip select (SRAM standard)	88	I	RXIN	Data receiving signal from PC
38	O	XINTRQ	Interrupt request output	89	O	XRTS	Sending of send-ready signal to PC
39	O	XREVSL	Chip select (spare)	90	O	XDSR	Sending of data terminal ready to PC
40	I	XRESET	System reset	91	I	XCTS	Sending request from PC
41	—	GND	Ground	92	I	XDTR	Data set ready sending to PC
42	I	CLKF	System clock	93	O	XRSCI	Call-back to PC
43	O	XCDCSL	Chip select	94	O	XRSCD	Carrier detection to PC
44	O	XGACSL1	Chip select (spare)	95	I	XRSOPT	PCI/F presence detection
45	O	XGACSL0	Chip select	96	O	RTCIO	RTC input/output control
46	O	XGABSL	Chip select (gate array B)	97	O	RTCCE	RTC chip select
47	O	XWR	System write output	98	O	RTCCK	RTC data transfer clock
48	I	XRD	System read signal	99	I/O	RTCDT	RTC data input/output
49	I	XWRH	System write (high-order byte) signal	100	—	VDD	Power supply
50	I	XWRL	System write (low-order byte) signal	101	—	GND	Ground
51	I/O	D15	System data input/output	102	O	PHIA	CCD clock A

LZ9FJ37A (IC14) Terminal descriptions

PIN	I/O	Name	Function	PIN	I/O	Name	Function
103	O	PHIB	CCD clock B	154	O	RA3	Reading memory address output
104	O	PHIR	CCD reset signal	155	O	RA4	Reading memory address output
105	O	XPHIT	CCD #T output	156	O	RA5	Reading memory address output
106	I	XA3FRS	Input port	157	O	RA6	Reading memory address output
107	I	XB4FRS	Input port	158	O	RA7	Reading memory address output
108	I	XFRSNS	Input port	159	O	XMDMRST	Modem reset output
109	I	XORGSNS	Input port	160	—	GND	Ground
110	I	XDRSNS	Input port				
111	O	XPHISH	Video sample hold				
112	O	XPHIBL	Line clamp				
113	O	HTEN	Half tone select output				
114	O	XGTW	Peak hold gate				
115	O	XPGST	Peak hold circuit clear				
116	O	ADCK	ADC sampling clock output				
117	I	B7	Video data input				
118	I	B6	Video data input				
119	I	B5	Video data input				
120	I	B4	Video data input				
121	—	GND	Ground				
122	I	B3	Video data input				
123	I	B2	Video data input				
124	I	B1	Video data input				
125	I	B0	Video data input				
126	O	RA12	Reading memory address output				
127	O	RA11	Reading memory address output				
128	O	RA10	Reading memory address output				
129	O	RA9	Reading memory address output				
130	O	RA8	Reading memory address output				
131	O	XRWE	Reading memory write output				
132	O	XROE	Reading memory read output				
133	I/O	RAD15	Reading memory data input/output				
134	I/O	RAD14	Reading memory data input/output				
135	I/O	RAD13	Reading memory data input/output				
136	I/O	RAD12	Reading memory data input/output				
137	I/O	RAD11	Reading memory data input/output				
138	I/O	RAD10	Reading memory data input/output				
139	I/O	RAD9	Reading memory data input/output				
140	I/O	RAD8	Reading memory data input/output				
141	—	GND	Ground				
142	—	VDD	Power supply				
143	I/O	RAD7	Reading memory data input/output				
144	I/O	RAD6	Reading memory data input/output				
145	I/O	RAD5	Reading memory data input/output				
146	I/O	RAD4	Reading memory data input/output				
147	I/O	RAD3	Reading memory data input/output				
148	I/O	RAD2	Reading memory data input/output				
149	I/O	RAD1	Reading memory data input/output				
150	I/O	RAD0	Reading memory data input/output				
151	O	RA0	Reading memory address output				
152	O	RA1	Reading memory address output				
153	O	RA2	Reading memory address output				

(7) Gate array (B) block

The block is composed of the gate array (B) and SRAM (2 KByte).

1) LR38292(IC18) -- pin-160, QFP (gate array B)

The device has the following functions.

① Printing data process
The image data of the page memory for printing is converted into 400 dpi, and the smoothing and contracting processes are applied.

② Printer (PCU) interface
The control of resetting and so on to PCU and the image data processed in Item ① above are synchronized with the signal (HSYNC) from PCU and are transmitted to PCU in the serial mode.

③ DMA controller
(a) The binary-coded data of the draft transmitted in the serial mode from the gate array (A) LZ9FJ37A(IC14) and read with the scanner are transmitted to the page memory.

(b) The image data which will be printed are read from the page memory, and the process ① is applied to transmit the data to PCU in the serial mode.

④ CODEC (HD813201F) interface
(a) The timing is controlled for CPU to get an access to CODEC.

(b) The timing is controlled for CODEC to get an access to the page memory.

⑤ DRAM controller
Since DRAM is used for the page memory, and the address, RAS and CAS are controlled and refresh-controlled.

⑥ Panel interface
The key input detection on the operation panel, LED lighting con-trol and LCD display control are executed.

2) LH5116NA-10 (IC22) -- pin-24, SOP (16-bit SRAM)

This SRAM is a line memory for the printing data process (resolution power conversion, smoothening and contracting to 404 dpi) of the gate array (B).

LR38292 (IC18) Terminal descriptions

Pin	Name	I/O	Function
20	VCC		Power supply
62	VCC		
100	VCC		
142	VCC		
16	GND		Ground
21	GND		
35	GND		
48	GND		
61	GND		
78	GND		
87	GND		
101	GND		
125	GND		
134	GND		
143	GND		
65	MANRESB	O	Manual reset signal
66	RESETB	I	Reset signal
89	A5	I	Address signal on the system side
90	A4		
91	A3		
92	A2		
93	A1		
70	D15	I/O	Data bus signal on the system side
71	D14		
72	D13		
73	D12		
74	D11		
75	D10		
76	D9		
77	D8		
79	D7		
80	D6		
81	D5		
82	D4		
83	D3		
84	D2		
85	D1		
86	D0		
88	CSB	I	Chip select signal of gate array LR38292
97	RDB	I	Read signal on the system bus side
98	WRB	I	Write signal on the system bus side
115	SHCK0B	O	Reversion output of clock (SHCK) from CPU
116	SHCK	I	Clock (19.6 MHz) from CPU
95	GAINTB	O	Interrupt request signal to CPU of gate array LR38292
94	CDCINTB	O	Reversion output (to CPU) of interrupt request signal from HD813201F
96	DREQ0B	O	Reversion output (to CPU) of DMA transfer request signal from HD813201F
99	RSTCDCB	O	Reset signal to HD813201F (Default: Low)
102	CDCINT	I	Interrupt request signal from HD813201F
103	BRQT	I	Bus right request signal of image bus from HD813201F
104	BACKB	O	Bus right permission signal of image bus to HD813201F
105	DRQ0	I	DMA transfer request signal from HD813201F
106	DACK0B	O	Acknowledge signal of DMA transfer to HD813201F
107	CSCDCB	I	Chip select signal to HD813201F
108	MDENB	I	Data enable signal of image bus from HD813201F
109	READY	O	Ready signal of image bus access to HD813201F
110	MAS	I	Address strobe signal of image bus of HD813201F

LR38292 (IC18) Terminal descriptions

Pin	Name	I/O	Function
111	MAENB	I	Address enable signal of image bus of HD813201F
112	CK16M	I	16 MHz clock input
113	RDCDC	O	Register read signal (active H) of HD813201F of CPU
114	RDCDCB	O	Register read signal (active L) of HD813201F of CPU
139	MA20	I	Address of image bus of HD813201F
138	MA19		
137	MA18		
136	MA17		
135	MA16		
133	MAD15	I/O	Address/data of image bus of HD813201F Input mode is selected when HD813201F gets an access to image bus (MAENB=L). Data bus to memory (page memory) is selected when gate array LR38292 gets an access to the image bus.
132	MAD14		
131	MAD13		
130	MAD12		
129	MAD11		
128	MAD10		
127	MAD9		
126	MAD8		
124	MAD7		
123	MAD6		
122	MAD5		
121	MAD4		
120	MAD3		
119	MAD2		
118	MAD1		
117	MAD0		
155	DA11	I/O	Address bus to memory of image bus (page memory) When HD813201F gets an access to the image bus, address of MA21 thru MA16, MAD15 thru MAD1 are converted to Row/Column address in the page memory (DRAM) and output. When gate array LR38292 gets an access to the image bus, Row/Column address is output to the page memory (DRAM).
154	DA10		
153	DA9		
152	DA8		
151	DA7		
150	DA6		
149	DA5		
148	DA4		
147	DA3		
146	DA2		
145	DA1		
144	DA0		
156	DWEB	O	Write signal to memory (page memory: DRAM) of image bus
157	RAS1B	O	RAS1 signal to memory (page memory: DRAM) of image bus
158	RAS0B	O	RAS0 signal to memory (page memory: DRAM) of image bus
159	CASB	O	CAS signal to memory (page memory: DRAM) of image bus
140	DRMSIZE	I	Setting of size of memory (page memory: DRAM) of image bus Low: 16 Mbits High: 12 Mbits
141	DRMTYPE	I	Setting of type of memory (page memory: DRAM) of image bus Low: Address 8-bit type High: address 12-bit type (Valid only for DRMSIZE=L. Don't care for DRMSIZE=H.)
67	STVDB	I	Serial scanner data valid range signal
68	SRVID	I	Serial scanner data
69	SCCLK	I	Serial scanner data transfer clock
51	PCURESB	O	Reset signal for printer unit
52	HSYNC	I	Main scanning synchronous signal from printer unit
53	EPRDYB	I	Communication ready signal from printer unit
54	PRRDYB	I	Printing operation ready signal of printer unit
55	TODB	I	Sub-scanning synchronous signal to printer unit

Pin	Name	I/O	Function
56	ETBSYB	I	Status sending signal of printer unit
57	CTBSYB	O	Command sending signal to printer unit
58	PRINTB	O	Printing start/continuation signal to printer unit
59	PDATA	O	Printing image data to printer unit
60	CPRDYB	O	Communication ready signal to printer unit
63	XIN	I	Clock input (quartz oscillator connection)
64	XOUT	O	Clock output (quartz oscillator connection)
38	LMA10	O	Address bus of line memory for smoothing/contracting
37	LMA9		
36	LMA8		
34	LMA7		
33	LMA6		
32	LMA5		
31	LMA4		
30	LMA3		
29	LMA2		
28	LMA1		
27	LMA0		
40	LMD7	O	Data bus of line memory for smoothing/contracting
41	LMD6		
42	LMD5		
43	LMD4		
44	LMD3		
45	LMD2		
46	LMD1		
47	LMD0		
39	LMWEB		
26	LD15	I/O	Control/data bus and LED on/off control signal to key scan and LCD driver on the operation panel
25	LD14		
24	LD13		
23	LD12		
22	LD11		
19	LD10		
18	LD9		
17	LD8		
15	LD7		
14	LD6		
13	LD5		
12	LD4		
11	LD3		
10	LD2		
9	LD1		
8	LD0		
160	SEN7	I	Key input detection signal of operation panel
1	SEN6		
2	SEN5		
3	SEN4		
4	SEN3		
5	SEN2		
6	SEN1		
7	SEN0		
49	MEMTST	I	Terminal for device test of integrated memory Low is set except in the device test mode.
50	TEST	I	Terminal for device test Low is set except in the device test mode.

(8) CODEC block

This block is composed of CODEC, LS374 and LS244 in order to de-modulate the contracted image data of the draft read with the scan-ner and the letter image transmitted in the DMA mode from the sys-tem memory.

1) HD813201F (IC19) ... pin-80, 6FP (CODEC)

It operates at 16 MHz corresponding to the ceramic oscillator (X4) of 16 MHz.

The image memory is commonly used as the page memory. The image data of the draft read with the scanner in the page memory is contracted by MMR, and is transferred to the system memory (DRAM: IC7) by the DMA transfer function of CPU. Moreover, the image data transferred in the DMA mode from the system memory are demodulated with MMR, and are developed into the page memory.

2) SN74LS374 (IC126) ... pin-20, SOP

The data hold time during writing from main CPU to HD813201F is as-sured.

3) SN74LS244 (IC128) ... pin-20, SOP

When the main CPU reads the inner register of HD813201F, it will read the data through this buffer.

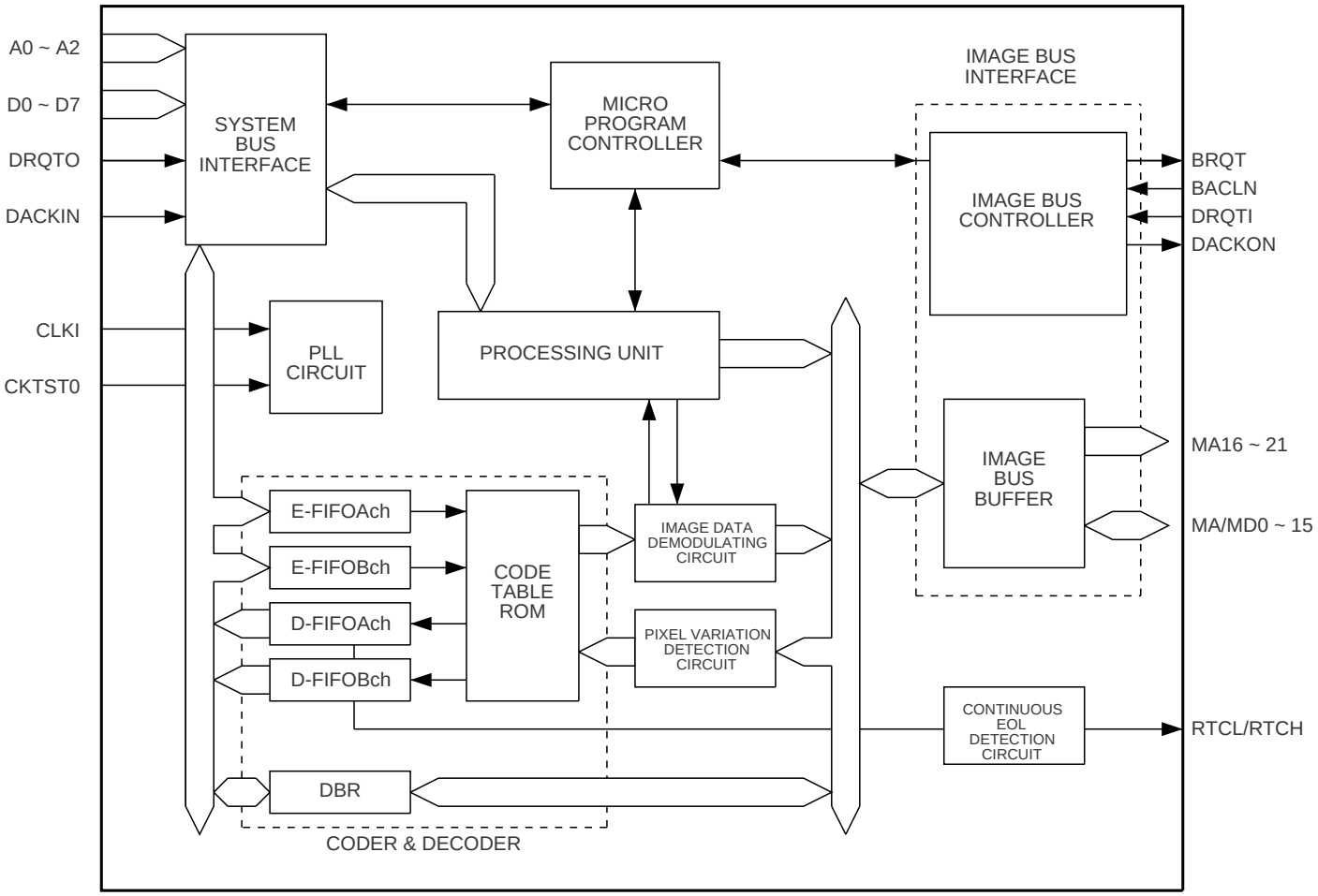


Fig. 2

HD813201F (IC19) Terminal descriptions

Code	Terminal No.	I/O	Function
$\overline{68}$/80	56	I	If this terminal is at "low" level, it indicates that MPU of system 88 is connected to IDP201. "High" level indicates that MPU of system 80 is connected.
A0	57	I	Addresses 0 thru 2 (address terminals). It is connected to the low-order 3 bits of the system address bus, and MPU is used to get an access to the internal register of IDP201.
A1	54		
A2	55		
D0	64	I/O, Three-state output	Data 0 thru 7 (data terminals). They are connected to the system data bus for bidirectional data transfer between MPU and IDP201. MPU can read and write the internal register of IDP201.
D1	62		
D2	65		
D3	63		
D4	67		
D5	66		
D6	68		
D7	69		
$\overline{CS}$	44	I	Chip select (chip select terminal). When the terminal is at "low" level, it indicates that MPU gets an access to the internal register of IDP201.
DS	45	I	Data strobe (data strobe terminal). Connect ϕ2 clock pin of MPU of system 88 or $\overline{RD}$ pin of MPU of system 80.
R/$\overline{W}$	42	I	Read/write (read/write terminal). Connect R/$\overline{W}$ pin of MPU of system 88 or $\overline{WR}$ pin of MPU of system 80.
$\overline{RESET}$	59	I	Reset element. If the signal of "low" level is input to the terminal, IDP201 will be initialized.
IRQT	58	O	Interrupt request (interrupt request terminal). When the signal of "high" level is output, IDP201 requests the interrupt process for MPU. The factor of the interrupt is the end of the command process, the end of DMA transfer, occurrence of an error during demodulation or the receiving of RTC code. MPU reads IRR (interrupt request register) which is one of the internal registers of IDP201, and can know the factor of the interrupt. When MPU reads IRR, IRQT becomes "low" level. (For details of IRR, refer to "8.1.2 Interrupt request register".)
DRQTO	47	O	DMA Request Output (DMA request output terminal). In the following cases, DMA transfer can be requested for DMAC by turning DRQTO to "high". (1) During coding, a code of 1 byte or more is stored in E-FIFO. (2) During decoding, an empty area of 1 byte or more is present. (3) During data transfer between the system bus and image bus, DBR is read to read or write.
$\overline{DACKI}$	46	I	DMA Acknowledge Input (DMA acknowledge input terminal) The response signal for DRQTO is input. If $\overline{DACKI}$ becomes "low" level during coding or decoding, the access is given to E-FIFO or D-FIFO. If $\overline{DACKI}$ becomes "low" level during data transfer between system bus and image bus, the access is given to DBR. Don't make $\overline{CS}$ and $\overline{DACKI}$ "low" at the same time.
BRQT	52	O	Bus Request (Bus request terminal). IDP201 outputs the signal of "high" level from BRQT, and IDP201 requests the bus master for the device which can become another bus master on the image bus. If any other device which can become the bus master on the image bus, BRQT becomes the NC pin.
$\overline{BACK}$	48	I	Bus Acknowledge (bus acknowledge terminal). The response signal for BRQT is input. If the signal of "low" level is input to $\overline{BACK}$, it indicates that it is approved for IDP201 to become the bus master of the image bus. If any other bus master which can become the bus master is not present except IDP201, fix this terminal at "low".
$\overline{MAEN}$	76	O	Memory Address Enable (Memory address enable terminal). IDP201 outputs the signal of "low" level from $\overline{MAEN}$ to declare that it becomes the bus master of the image bus. When $\overline{MAEN}$ is at "high", the three-state output which is connected to the image bus becomes all into the high impedance state.

HD813201F (IC19) Terminal descriptions

Code	Terminal No.	I/O	Function
MAS	74	O	Memory Address Strobe (Memory address strobe terminal). When MAS becomes "high" level, it indicates that address is output to MA/MD0 thru MA/MD15 and MA16 thru MA21.
UDS	27	Three-state output	Upper Data Strobe (high-order data strobe terminal). When $\overline{\text{UDS}}$ becomes "low" level, it indicates that IDP201 uses the high-order byte of the image bus.
$\overline{\text{LDS}}$	23	Three-state output	Upper Data Strobe (low-order data strobe terminal). When $\overline{\text{LDS}}$ becomes "low" level, it indicates that IDP201 uses the low-order byte of the image bus.
$\overline{\text{MDEN}}$	25	O	Memory Data Bus Enable (Memory data bus enable terminal). When $\overline{\text{MDEN}}$ output terminal becomes "low" level, it indicates that valid data are present in MA/MD0 thru MA/MD15. This output terminal is used to control the output of the bidirectional bus buffer on MA/MD0 thru MA/MD15.
MA/MD 0	79	I/O, Three-state output	Memory Address Data Bus 0 thru 15 (Memory address data bus). In this bus for image bus operation, the address and data are multiplexed. MA/MD0 thru MA/MD15 are used as follows. (1) When $\overline{\text{MAEN}}$ is "low" and MAS is "high", it is used as the output address line. (2) When both $\overline{\text{MAEN}}$ and $\overline{\text{MDEN}}$ are "low" in the reading cycle, it is used as the input data line. (3) When both $\overline{\text{MAEN}}$ and $\overline{\text{MDEN}}$ are "low" in the writing cycle, it is used as the input data line.
MA/MD 1	77		
MA/MD 2	3		
MA/MD 3	78		
MA/MD 4	5		
MA/MD 5	2		
MA/MD 6	6		
MA/MD 7	4		
MA/MD 8	8		
MA/MD 9	7		
MA/MD10	12		
MA/MD11	9		
MA/MD12	14		
MA/MD13	13		
MA/MD14	15		
MA/MD15	16		
MA16	71	Three-state output	Memory Address Bus 16 thru 21 (memory address bus). When $\overline{\text{MAEN}}$ is "low" and MAS is "high", it is used as the output address line.
MA17	11		
MA18	30		
MA19	31		
MA20	50		
MA21	51		
$\overline{\text{MR}}$	26	Three-state output	Memory Read (Memory read terminal). When $\overline{\text{MR}}$ is turned to "low" level, IDP201 reads the data from the image memory.
$\overline{\text{MW}}$	28	Three-state output	Memory Write (memory write terminal). When $\overline{\text{MW}}$ is turned to "low" level, IDP201 writes the data in the image memory.
$\overline{\text{IOR}}$	35	Three-state output	I/O Read (I/O read terminal). When $\overline{\text{IOR}}$ is turned to "low" level, IDP201 reads the data from I/O device on the image bus. However, it is limited at DMA transfer during data transfer with the transfer command and the coding process.
$\overline{\text{IOW}}$	36	Three-state output	I/O Write (I/O write terminal). When $\overline{\text{IOW}}$ is turned to "low" level, IDP201 writes the data in I/O device on the image bus. However, it is limited at DMA transfer during data transfer with the transfer command and the decoding process.
DRQTI	39	I	DMA Request Input (DMA request input terminal). When I/O device on the image bus requests DMA for IDP201, DRQTI becomes "high" level.
$\overline{\text{DACKO}}$	38	O	DMA Acknowledge Output (DMA acknowledge output terminal). When this output terminal is turned to "low" level, IDP201 informs to the peripheral devices on the image bus that DMA operation is approved.
$\overline{\text{DMA}}$	32	O	Direct Memory Access (Direct memory access terminal). When $\overline{\text{DMA}}$ output is turned to "low", it indicates that DMA transfer is executed. In the coding process, the data is transferred from the I/O device (scanner) to the image memory. In the decoding process, the data is transferred from the image memory to I/O device (printer).

HD813201F (IC19) Terminal descriptions

Code	Terminal No.	I/O	Function
DTC	37	O	DMA Terminal Count (DMA terminal count terminal). When DTC output is turned to "high", it indicates that DMA transfer of the setting line part is ended.
READY	73	I	Image memory or I/O device read. When READY is turned to "high" during writing, it indicates that the image memory or I/O device is ready for transmitting/receiving the data. When READY is "high", IDP201 will wait until READY becomes "high".
<Power terminal>			
V_{DD} 1	29	I	Power voltage (+5V)
V_{DD} 2	49	I	
V_{DD} 3	72	I	
V_{SS} 1	10	I	
V_{SS} 2	17	I	Ground
V_{SS} 3	34	I	
V_{SS} 4	53	I	
V_{SS} 5	70	I	
V_{SS} 6	75	I	
<Other>			
TEST 0	18	I	Fix these terminals at "low".
TEST 1	22	I	
TEST 2	24	I	
TEST 3	33	I	
TEST 4	43	I	

Code	Terminal No.	I/O	Name and function
CLKI	19	I	Quartz oscillation input terminal and external clock input terminal
CLKX	20	O	Quartz oscillation output terminal
CKTST1	1	I	Low pass filter terminal of PLL circuit Connected to capacitor (1000pF) and resistor (10kΩ) through GND.
CLKMOD	40	I	Terminal to switch quartz oscillation connection or external clock input mode. "0": Quartz oscillation "1": External clock
CKTST0	41	I	Fix at "LOW" level.
CLKO	21	O	Clock output terminal. Rectangular wave which is synchronous with the internal clock of IDP201 is output.
CKTST2	80	I	Fix at "LOW" level.

Code	Terminal No.	I/O	Name and function
RTCH	60	O	Number of transfers of EOL detected by IDP201 during RTC receiving is reflected at the terminal.
RTCL	61	O	

(9) Page memory block

The page memory block is composed of one DRAM of 1M × 16 bits, being commonly used as the image memory. The memory is divided into the page memory for the scanner and the page memory for printing.

The page memory for scanner is composed of the whole area of IC12. The image data of approx. one page (except in the super fine mode) of the draft read with the scanner can be stored. They are stored until they are contracted by CODEC.

The page memory for printing is composed of the remaining areas of IC12 and can store approx. one page of the image data decoded by CODEC. The data are stored until they are transferred to PCU with the gate array (B) and printed.

(10) Driver block

Sending motor driver (IC20, IC21: PBL3717/2) ---- 16-pin DIP
This IC drives at the sending motor at the constant current with the bipolar, chopper system.

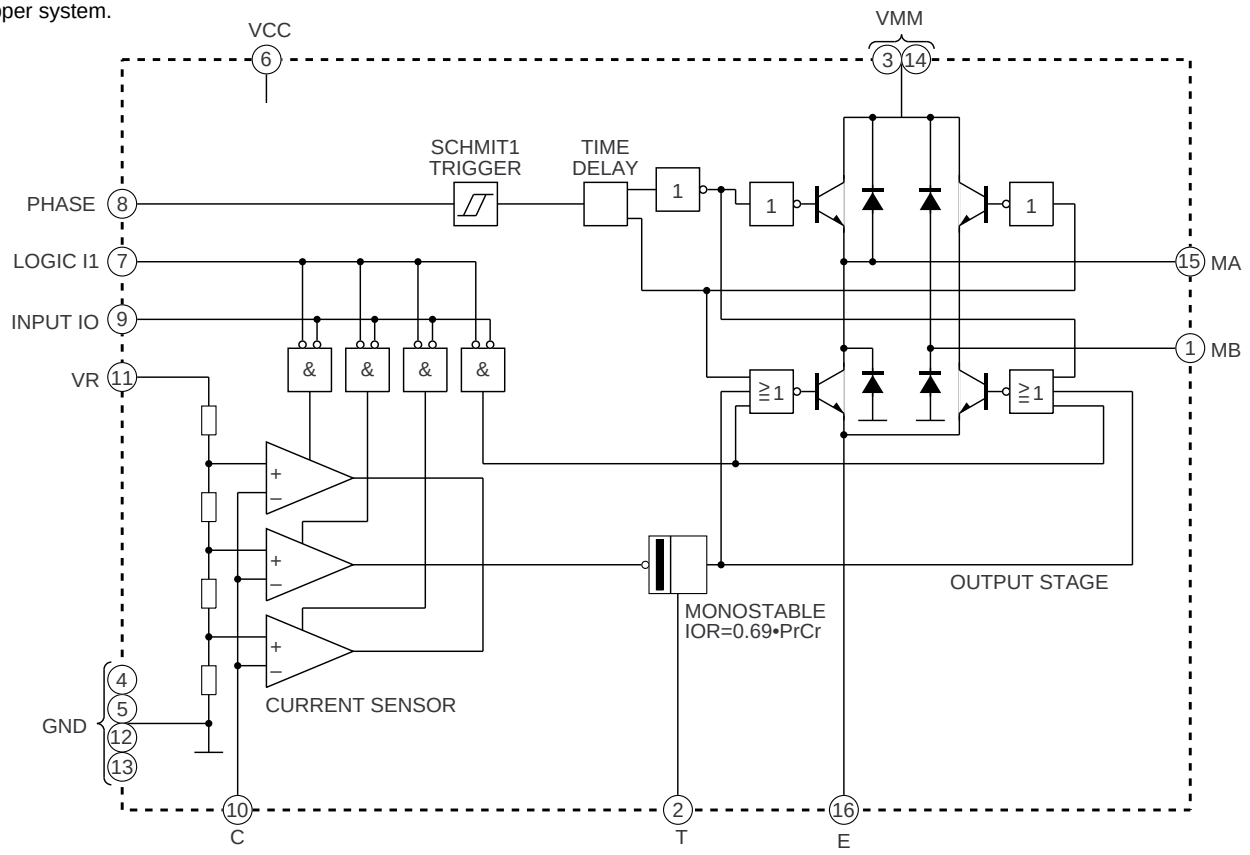


Fig. 3

- Operation description (Refer to the waveforms of the terminal voltage and current waveforms.

① The current M in the coiling of the motor is converted in the current-voltage mode with the resistors RS (R1, 2) which are connected the terminal E (pin 16), is farther transmitted to the C terminal (pin 10) through the filter Cc (C248, 252) and Rc (R399, 401). (Vc)

② The reference voltage (VR') and (Vc) voltage of each comparator are compared with the comparator which is selected with I_0 (pin 9) and I_1 (pin 7).

③ If Vc ≥ VR' is established here, the signal is output to the monostable to turn off the lower side of the bridge type output transistor only for the time (0.69CrRr) determined by CT (C251, 255) and RT (R400, 402) which are connected to the terminal T (pin 2) in order to shut down the coil current IM.

④ At this time, the counter-electromotive force is generated by the winding inductance. However, the energy is reduced with discharge through V_{MM} and the diode between M_A and M_B.

⑤ When the time (0.69CrRr) determined with the monostable has passed, the transistor on the lower side is turned on again to flow the winding current I_M. Being suppressed by the inductance of the motor, the current will increase and return to ① .

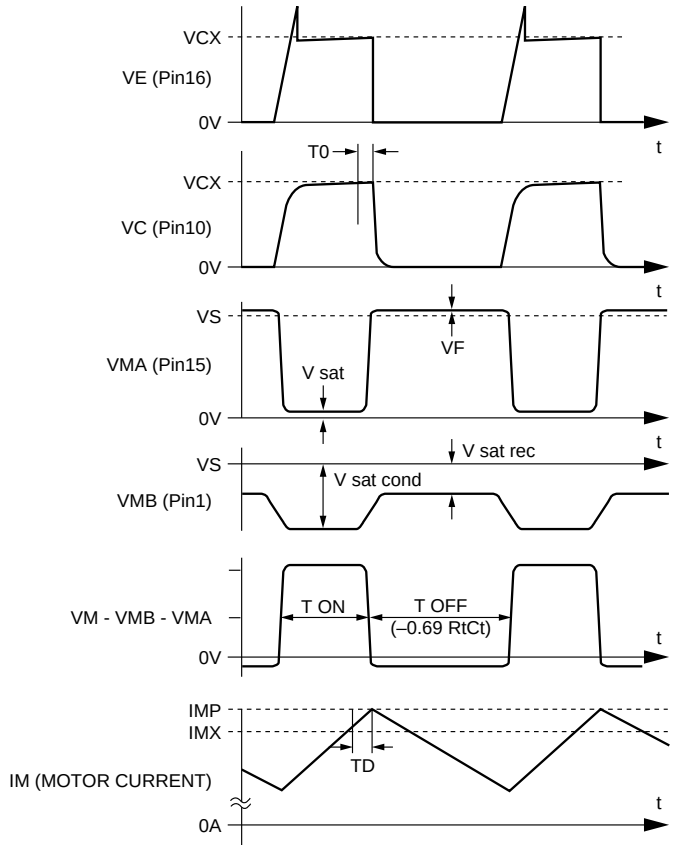


Fig. 4

LH28F016SUT (IC6) Terminal descriptions

Symbol	Type	Name and function
A0	I	Byte select address: The device selects the low-order or high-order byte in the ×8 mode. Not used in the ×16 mode. (The A_0 input circuit is not activated since Byte # is high.)
A_1 - A_{15}	I	Word select address: One word is selected in the 64 KByte block. These addresses are latched in the data writing operation.
A_{16} - A_{20}	I	Block select address: 1/32 erasion block is selected. These addresses are latched when data writing, erasion or lock block is activated.
DQ_0 - DQ_7	I/O	Low-order byte data input/output: Data and command input in the command user interface writing cycle. When various data are read, the memory array, page buffer, identifier and status data are output. It is floated when the chip is not selected or output is disable.
DQ_8 - DQ_{15}	I/O	High-order byte data input/output: Same function as the low-order byte data input/output. Operable in the ×16 mode alone. It is floated in the ×8 mode.
CE_0#, CE_1#	I	Chip enable: The control logic, input butter, decoder and sense amplifier are made to be active. The chip is active only when both CE_0# and CE_1# are at "low".
RP#	I	Reset/power down: The device is brought into the deep power down state when RP# is turned to "Low". In order to recover it from the deep power down state, 400ns (ordinary lead time of +5ns for reading) is necessary. When RP# pin becomes "low", all chip operations are interrupted and reset.
OE#	I	Output enable: Data is output from DQ pin by turning OE# to "Low". When OE# is turned to "High", DQ pin is floated.
WE#	I	Write enable: The accesses to the command user interface, buffer, data cue register and address cue latch are controlled. When WE# is "Low", it becomes active to fetch the address and data at the leading edge.
RY/BY#	O	Ready/busy: The status of the internal write state machine is output. "Low" indicates that the write state machine is in operation. RY/BY# pin is floated when the write state machine waits for instruction of next operation, erasion is interrupted or it is in the deep power down state.
WP#	I	Write protect: Each block can be protected from writing/erasion by writing data into the no-volatile lock bit of the block. Writing/erasion becomes impossible for the block in which WP# is "low" and the block lock status bit (BSR.6) is protected. If WP# is "High", writing/erasion is possible regardless of the status of the lock bit. When RP# is "low" (in the deep power down state), WP# input circuit becomes disable.
BYTE#	I	Byte enable: When BYTE# is turned to "Low", the device is brought into the ×8 mode. At this time, DQ8-DQ15 becomes floated. The address A0 selects the high-/low-order byte. When BYTE# is "High", the device is brought into the ×16 mode, and the A0 input circuit becomes disable.
3/5#	I	3.3V/5.0V: When 3/5# is "High", the internal circuit can be operated at 3.3V, and when 3/5# is "Low", the internal circuit can be operated at 5.0V. * Note: If 3/5# is turned to "High" when 5V is applied to Vcc, the device may be broken.
Vpp		Writing/erasion power: 5.0±0.5V is applied during writing/erasion.
Vcc		Device power: 5.0±0.5V or 3.3±0.3V
GND		Ground
NC		Not connected.

LH28F016SUT (IC6)

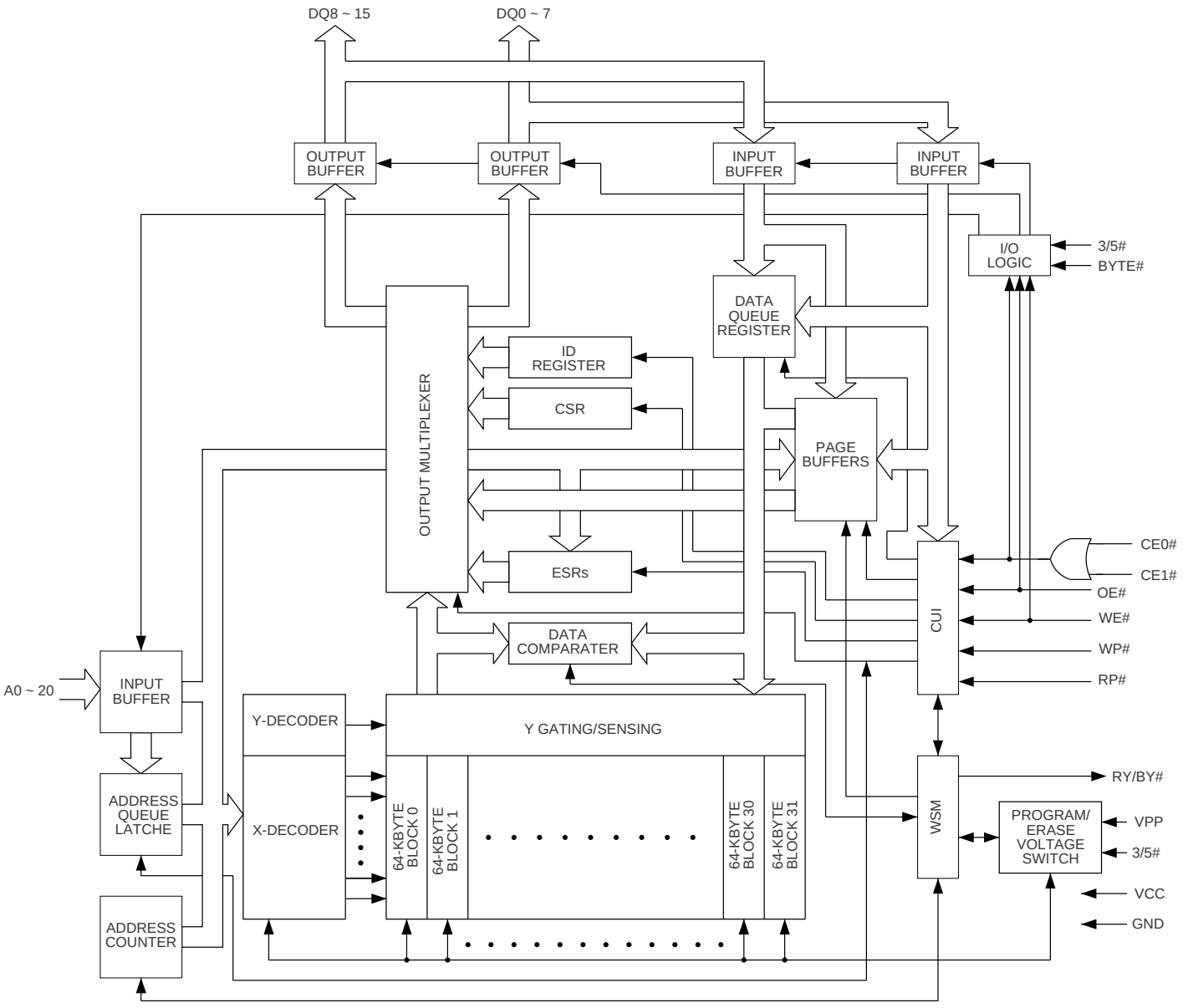
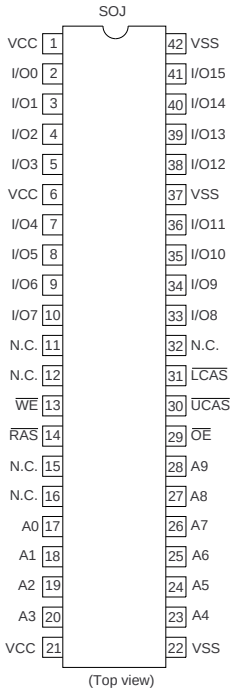


Fig. 5

HM5118160AF-7 (IC12)



Pin name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
I/O0 to I/O15	Data-in/Data-out
$\overline{RAS}$	Row address strobe
$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
Vcc	Power supply
Vss	Ground
N.C	No connection

Fig. 6

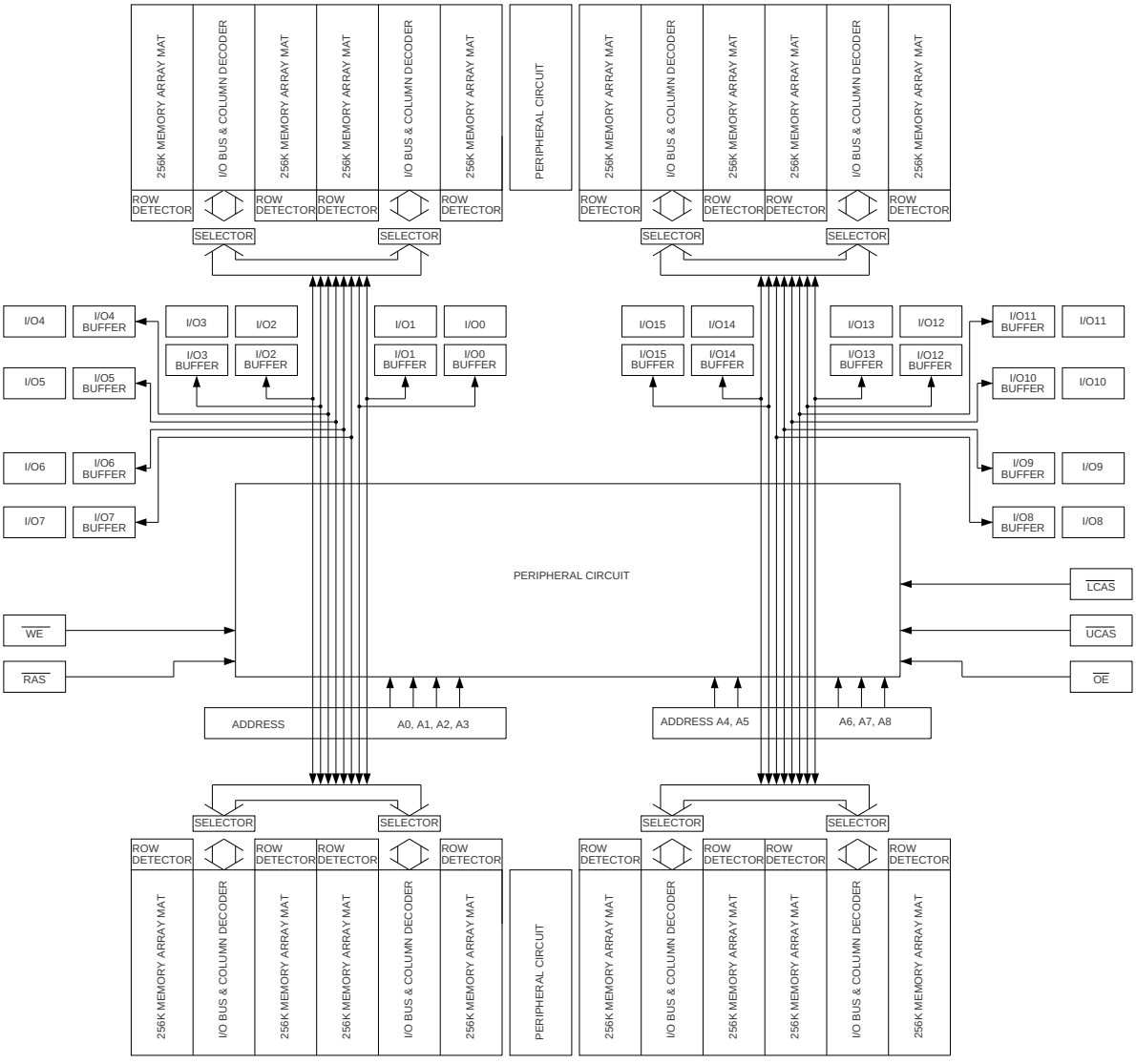


Fig. 7

(11) Connector block (CNSB)

- CNSB of 50 pin connector connect the control PWB with the line control PWB.
- Speaker sound control

  Output of the circuit monitor sound, key input sound, alarm sound and ringer sound is switched with the analog switch (IC119: BU4053), and the sound volume is controlled with the analog switch (IC116: NJU4051).

(12) Access control block

This block control the with access to the dual port RAMs of sub-1 or sub-2.

(13) Sub-1 CPU block

The main control block uses RISC microprocessor HD6437021 as CPU, being composed of ROM (1 MByte) and DRAM (512 KByte).

1) HD6437021 (IC14): pin-100, QFP (main CPU)

The device is a microprocessor which integrates the peripheral functions, using CPU of 32-bit RISC type as the core. In the instrument, the following peripheral functions are mainly used.

① ROM of 32 KByte and RAM of 1 KByte are integrated.
A part of programs are stored in the integrated ROM.

② DMA controller (4 channels are provided, and 2 channels alone are used.)
ch.0: Used to transmit image data between CODEC (HM514260) and DRAM(IC15).
ch.3: Used to transmit image data between CPU and DRAM(IC15).

③ Clock-synchronous type serial communication interface Commands and statuses are communicated with PCU.

④ Start-stop synchronous type serial communication interface Used for PC interface of RS232C system.

⑤ Interruption

$\overline{IRQ6}$: Interruption request from gate array (A) (LZ9FJ37A)

$\overline{IRQ7}$: Interruption request from gate array (B) (LR38292)

$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQ3}$, $\overline{IRQ4}$, $\overline{IRQ5}$: Not used.

$\overline{NMI}$: Not used.

⑥ DRAM controller
Addressing to DRAM(IC15) of the system and control and refresh control of $\overline{RAS}$ and $\overline{CAS}$ signals are executed.

⑦ Timer and watch dog timer

⑧ General-purpose I/O port
Control of TEL/Liu are executed.

⑨ Clock oscillation
Ceramic oscillator of 19.66 MHz is connected for operation of 19.66 MHz.

(14) Sub-1 ROM, DRAM block

1) 27C4002 (IC10): pin-40, DIP (ROM)

Programs are stored in two 4 Mbit ROM.

2) HM514260 (IC15): pin-40, SOJ (DRAM)

Used as the system memory of main CPU and transmission buffer of communication.

(15) Dual port RAM-1 block

Dual port RAMs allow main CPU and sub-1 CPU to communicate with each other by passing data through the common memory.

1) IDT7130 (IC16)

2) IDT7140 (IC17)

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory.

(16) Connector block (CNLIU)

CNLIU of 26 pin connector connect the control PWB with the TEL/LIU 1 PWB.

(17) Sub-1 access control block

The block control the write access to the dual port RAMs (IC16, 17) and the modem (IC3).

[3] Circuit description of line control PWB

1. General description

The line control PWB is composed of the following blocks.

① Sub-2 CPU block
② Modem-2 block
③ Sub-2 EPROM, DRAM block
④ Dual port RAM-2 block
⑤ Connector block (CNLIU1/CNSB1)
⑥ Sub-2 access control block

(1) Sub-2 CPU block

The main control block uses RISC microprocessor HD6437021 as CPU, being composed of ROM (1 MByte) and DRAM (512 KByte).

1) HD6437021 (IC7): pin-100, QFP (main CPU)

The device is a microprocessor which integrates the peripheral functions, using CPU of 32-bit RISC type as the core. In the instrument, the following peripheral functions are mainly used.

① ROM of 32 KByte and RAM of 1 KByte are integrated.
A part of programs are stored in the integrated ROM.

② DMA controller (4 channels are provided, and 2 channels alone are used.)
ch.0: Used to transmit image data between CODEC (HM514260) and DRAM(IC3).
ch.3: Used to transmit image data between CPU and DRAM(IC3).

③ Clock-synchronous type serial communication interface Commands and statuses are communicated with PCU.

④ Start-stop synchronous type serial communication interface Used for PC interface of RS232C system.

⑤ Interruption

$\overline{IRQ6}$: Interruption request from gate array (A) (LZ9FJ37A)

$\overline{IRQ7}$: Interruption request from gate array (B) (LR38292)

$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQ3}$, $\overline{IRQ4}$, $\overline{IRQ5}$: Not used.

$\overline{NMI}$: Not used.

⑥ DRAM controller
Addressing to DRAM(IC3) of the system and control and refresh control of $\overline{RAS}$ and $\overline{CAS}$ signals are executed.

⑦ Timer and watch dog timer

⑧ General-purpose I/O port
Control of TEL/Liu are executed.

⑨ Clock oscillation
Ceramic oscillator of 19.66 MHz is connected for operation of 19.66 MHz.

(2) Modem-2 block

The block is mainly composed of the modem R288F (IC8), and is provided with the following modem function.

Configuration	Modulation 1	Carrier Frequency (Hz) ± 0.01 %	Data Rate (bps) ± 0.01 %	Symbol Rate (Symbols/Sec.)	Bits/Symbol-Data	Bits/Symbol-TCM	Constellation Points
V. 34 33600 TCM	TCM	Note 2	33600	3429 only	Note 2	Note 2	Note 2
V. 34 31200 TCM	TCM	Note 2	31200	Note 2	Note 2	Note 2	Note 2
V. 34 28800 TCM	TCM	Note 2	28800	Note 2	Note 2	Note 2	Note 2
V. 34 26400 TCM	TCM	Note 2	26400	Note 2	Note 2	Note 2	Note 2
V. 34 24000 TCM	TCM	Note 2	24000	Note 2	Note 2	Note 2	Note 2
V. 34 21600 TCM	TCM	Note 2	21600	Note 2	Note 2	Note 2	Note 2
V. 34 19200 TCM	TCM	Note 2	19200	Note 2	Note 2	Note 2	Note 2
V. 34 16800 TCM	TCM	Note 2	16800	Note 2	Note 2	Note 2	Note 2
V. 34 14400 TCM	TCM	Note 2	14400	Note 2	Note 2	Note 2	Note 2
V. 34 12000 TCM	TCM	Note 2	12000	Note 2	Note 2	Note 2	Note 2
V. 34 9600 TCM	TCM	Note 2	9600	Note 2	Note 2	Note 2	Note 2
V. 34 7200 TCM	TCM	Note 2	7200	Note 2	Note 2	Note 2	Note 2
V. 34 4800 TCM	TCM	Note 2	4800	Note 2	Note 2	Note 2	Note 2
V. 34 2400 TCM	TCM	Note 2	2400	Note 2	Note 2	Note 2	Note 2
V. 23 1200/75	FSK	1700/420	1200/75	1200	1	0	—
V. 21	FSK	1080/1750	0-300	300	1	0	—
V. 17 14400 TCM	TCM	1800	14400	2400	6	1	128
V. 17 12000 TCM	TCM	1800	12000	2400	5	1	64
V. 17 9600 TCM	TCM	1800	9600	2400	4	1	32
V. 17 7200 TCM	TCM	1800	7200	2400	3	1	16
V. 29 9600	QAM	1700	9600	2400	4	0	16
V. 29 7200	QAM	1700	7200	2400	3	0	8
V. 29 4800	QAM	1700	4800	2400	2	0	4
V. 27 4800	DPSK	1800	4800	1600	3	0	8
V. 27 2400	DPSK	1800	2400	1200	2	0	4
V. 21 Channel 2	FSK	1750	300	300	1	0	—

Notes:

1. Modulation legend: TCM: Trellis-Coded Modulation QAM: Quadrature Amplitude Modulation
   FSK: Frequency Shift Keying DPSK: Differential Phase Shift Keying
2. Adaptive; established during handshake:

	Carrier Frequency (Hz)	
Symbol Rate (Baud)	V. 34 Low Carrier	V. 34 High Carrier
2400	1600	1800
2800	1680	1867
3000	1800	2000
3200	1829	1920
3429	1959	1959

(3) Sub-2 ROM, DRAM block

1) 27C4002 (IC6): pin-40, DIP (ROM)

Programs are stored in two 4 Mbit ROM.

2) HM514260 (IC3): pin-40, SOJ (DRAM)

Used as the system memory of main CPU and transmission buffer of communication.

(4) Dual port RAM-2 block

Dual port RAMs allow main CPU and sub-2 CPU to communicate with each other by passing data through the common memory.

1) IDT7130 (IC11)

2) IDT7140 (IC12)

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory.

(5) Connector block (CNLIU1/CNSB1)

- CNLIU1 of 26 pin connector connect the control PWB with the TEL/LIU 2 PWB.
- CNSB1 of 50 pin connector connect the control PWB with the line control PWB.

(6) Sub-2 access control block

The block control the write access to the dual port RAMs (IC11, 12) and the modem (IC8).

[4] Circuit Description of TEL/LIU 1 PWB

(1) TEL/LIU block operational description

1) Block diagram

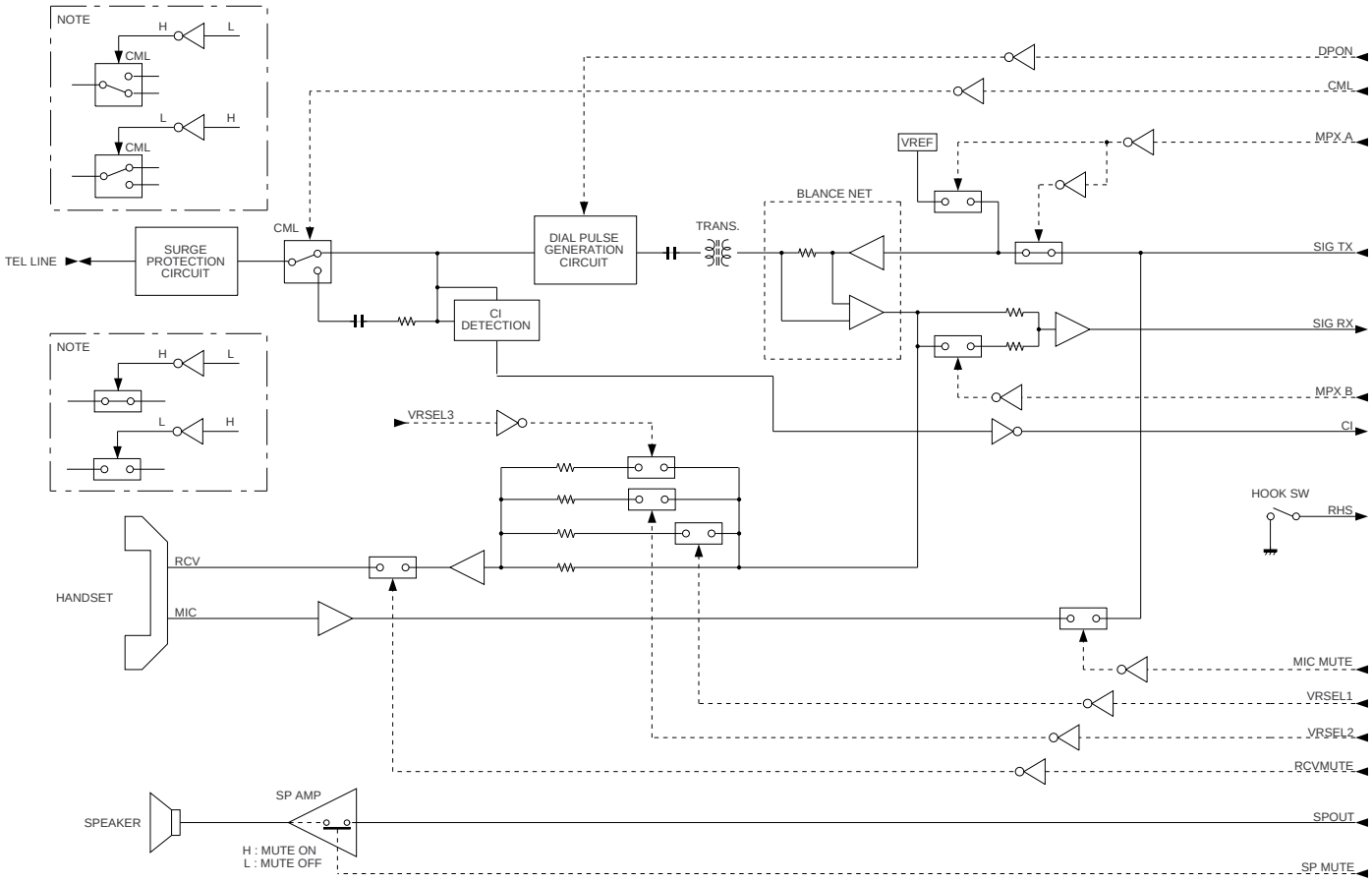


Fig. 8

2) Circuit description

The TEL/LIU PWB is composed of the following 12 blocks.

1. Surge protection circuit
2. Noise filter
3. On-hook status detection circuit
4. Dial pulse generation circuit
5. CML relay
6. Matching transformer
7. Hybrid circuit
8. Speaker amplifier
9. Adjustment of voice volume
10. Signal selection
11. CI detection circuit
12. Power supply and bias circuit

3) Block description

1. Surg Protection circuit

This circuit protects the circuit from the surge voltage occurring on the telephone line.

- The AR1 protects the circuit from the 390V or higher line surge voltages.
- The VA1 and VA2 protect the circuit from the 470V or higher vertical surge voltages.
- The ZD4 and ZD5 control the voltages generated on the secondary side of matching transformer to 2V.
- The VA3 protect the circuit from 100V or higher line surge voltages.

2. Noise filter

The noise filter comprises the RF choke coil, L1, L2, L3 and capacitor C16.

- The L1, L2, L3 and C16 prevent unnecessary radio noises from being transmitted from the telephone line.
- The C16 prevent radio pickup from the telephone line.

3. On-hook status detection circuit

The hook status detection circuit detects the Status of hook switch (RHS) of the Built-in telephone.

- The status of on-hook switch (RHS) is determined from the logical level of $\overline{\text{RHS}}$ signal.
  $\overline{\text{RHS}}$ LOW: OFF HOOK
  $\overline{\text{RHS}}$ HIGH: ON HOOK

4. Dial pulse generation circuit

The pulse dial generation circuit comprises of the photo-coupler PC2, polarity guard REC1, and transistor Q1, Q2.
The dial pulse turns on CML, controls the base current of transistor Q2 by supplying the DP signal to the photo-coupler PC2, and generates the DP signal by making the TEL circuit make and break.

5. CML relay

The CML relay switches over connection to the matching transformer T1 while the FAX or built-in telephone is being used.

6. Matching transformer

The matching transformer provides electrical insulation from the telephone line and impedance matching for transmitting the TEL/FAX signal.

7. Hybrid circuit

The hybrid circuit performs 2-wire-to-4-wire conversion using the IC105 and IC104 of the operational amplifier, transmits the voice transmission signal to the line, and feeds back the voice signal to the voice reception circuit as the side tone. Also, this circuit is operated with the analog switch IC104 as a half-duplex circuit while the FAX is being used, and as a full-duplex circuit while the telephone is being used.

The C11, C115, C120, C116 and C112 suppress the radio pickup from the handset.

8. Speaker amplifier

The speaker amplifier monitors the line under the on-hook mode, outputs the buzzer sound generated from the gate array (IC11: control PWB), ringer sound, DTMF generated from the modem (IC1: control PWB), and line sound.

9. Adjustment of voice volume

The voice volume can be adjusted by using the panel bottons "→" and "←".

- The reception level can be adjusted by pressing the →/← button when the handset is located in the off-hook state.

10. Signal selection

The following signals are used to control the transmission line of TEL/FAX signal. For details, refer to the signal selector matrix table. (See page 5-29)

- TEL MUTE: Controls the mute of handset voice transmission signal.
- RCV MUTE: Controls the mute of handset voice reception signal.
- SP MUTE: Controls the mute of speaker amplifier.
- MPX B: Switches over the gain of reception amplifier.
  H: Amplifier gain decreased
  L: Amplifier gain increased
- MPX A: Mutes the transmission drive amplifier.
  H: Selected when the telephone is being used or when the FAX signal is being transmitted
  L: Selected when the FAX signal is being received

11.CI detection circuit

The CI detection circuit detects the CI signals of 15.3 Hz to 68 Hz. A CI signal, which is provided to the photo-coupler PC1 through the C15 (0.82 μF), R1 (22 K), R2 (13K) and ZD3 when the ring signal is inputted from the telephone line, is filtered by the R137 and C9 and then transmitted to the control PWB through the Q110 (DTC114).

12. Power supply and bias circuits

The voltages of +12V and +5V are supplied from the control PWB unit. The IC104 of operational amplifier generates 6V bias voltage and supplies it to the IC104, 106, 105.

(Example: Fax signal send)

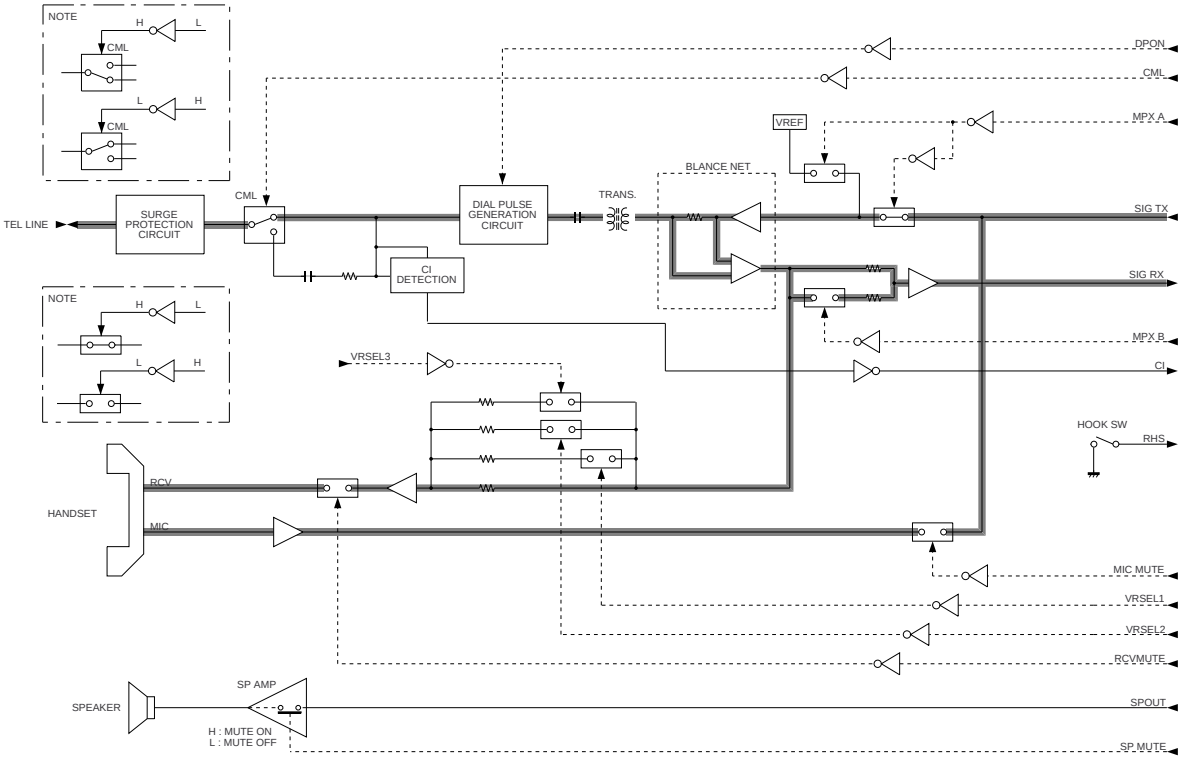


Fig. 9

Matrix table of control signals

		CML	MPXA	MPXB	MIC MUTE	RCV MUTE	SP MUTE
		H: ON L: OFF	H: TX LINE L: OFF	H: Low gain L: High gain	H: ON L: OFF	H: ON L: OFF	H: ON L: OFF
Stand-by		L	L	L	H	H	H
FAX signal sending		H	H	H	H	H	H
FAX signal receiving		H	L	H	H	H	H
Off-hook dial	Before and after dialing	H	H	H	L	L	H
	DP dialing	L	L	H	H	L	H
	DTMF dialing	H	H	H	H	L	H
On-hook dial	Before and after dialing	H	L	H	L	H	L
	DP dialing	L	L	L	H	H	L
	DTMF dialing	H	H	H	H	H	L
Auto dial	Before and after dialing	H	L	H	H	H	H
	300bps check	H	L	H	H	H	H
	DP dialing	L	L	H	H	H	H
	DTMF dialing	H	H	H	H	H	H
Ringer ringing		L	L	L	H	H	L
Key buzzer	Stand by/buzzer	L	L	L	H	H	L
	OFF HOOK	H	H	H	L	L	L
	ON HOOK	H	H	H	H	H	L
Holding	ON HOOK	H	H	H	H	H	L
	OFF HOOK	H	H	H	H	H	H

Sound volume control signal of hand-set receiver

VRSEL1/VRSEL2/VRSEL3 Matrix

Sound volume	High	Middle	Low	DTMF sending
VRSEL 1	L	H	H	H
VRSEL 2	H	L	H	H
VRSEL 3	H	H	L	H

[5] Circuit Description of TEL/LIU 2 PWB

(1) TEL/LIU block operational description

1) Block diagram

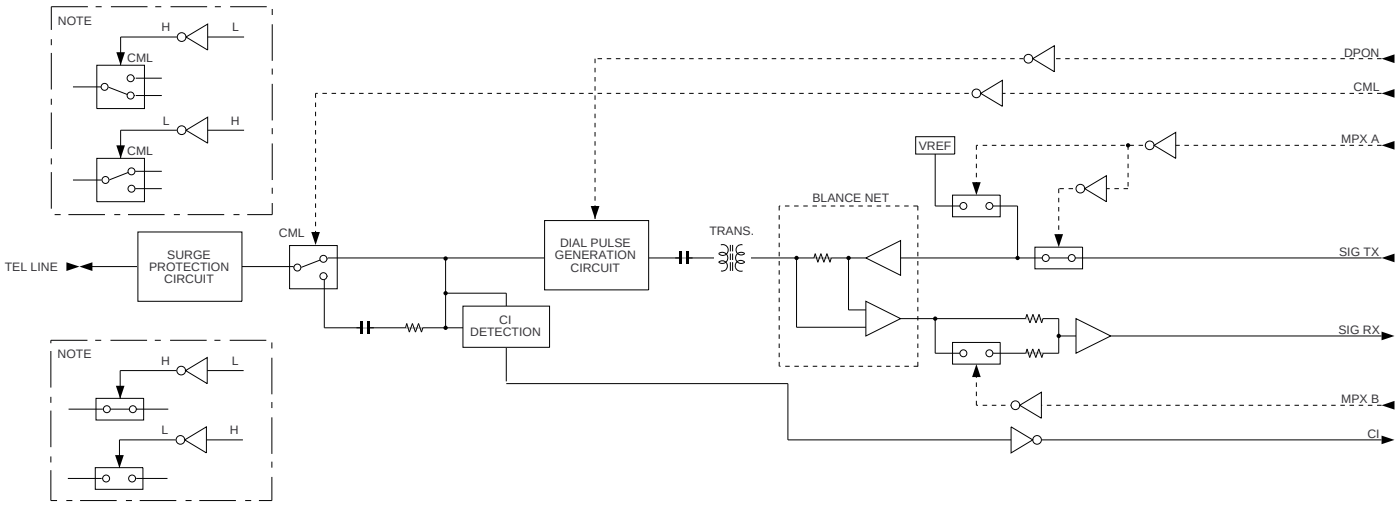


Fig. 10

2) Circuit description

The TEL/LIU PWB is composed of the following 9 blocks.

1. Surge protection circuit
2. Noise filter
3. Dial pulse generation circuit
4. CML relay
5. Matching transformer
6. Hybrid circuit
7. Signal selection
8. Cl detection circuit
9. Power supply and bias circuit

3) Block description

1. Surg Protection circuit

This circuit protects the circuit from the surge voltage occurring on the telephone line.

- The AR1 protects the circuit from the 390V or higher line surge voltages.
- The VA1 and VA2 protect the circuit from the 470V or higher vertical surge voltages.
- The ZD4 and ZD5 control the voltages generated on the secondary side of matching transformer to 2V.
- The VA3 protect the circuit from 100V or higher line surge voltages.

2. Noise filter

The noise filter comprises the RF choke coil, L1, L2, L3 and capacitor C16.

- The L1, L2, L3 and C16 prevent unnecessary radio noises from being transmitted from the telephone line.
- The C16 prevent radio pickup from the telephone line.

3. Dial pulse generation circuit

The pulse dial generation circuit comprises of the photo-coupler PC2, polarity guard REC1, and transistor Q1, Q2.

The dial pulse turns on CML, controls the base current of transistor Q2 by supplying the DP signal to the photo-coupler PC2, and generates the DP signal by making the TEL circuit make and break.

4. CML relay

The CML relay switches over connection to the matching transformer T1 while the FAX or built-in telephone is being used.

5. Matching transformer

The matching transformer provides electrical insulation from the telephone line and impedance matching for transmitting the TEL/FAX signal.

6. Hybrid circuit

The hybrid circuit performs 2-wire-to-4-wire conversion using the IC105 and IC104 of the operational amplifier, transmits the voice transmission signal to the line, and feeds back the voice signal to the voice reception circuit as the side tone. Also, this circuit is operated with the analog switch IC104 as a half-duplex circuit while the FAX is being used, and as a full-duplex circuit while the telephone is being used.

The C11, C115, C120, C116 and C112 suppress the radio pickup from the handset.

7. Signal selection

The following signals are used to control the transmission line of TEL/FAX signal. For details, refer to the signal selector matrix table. (See page 5-29)

- MPX B: Switches over the gain of reception amplifier.
  - H: Amplifier gain decreased
  - L: Amplifier gain increased
- MPX A: Mutes the transmission drive amplifier.
  - H: Selected when the telephone is being used or when the FAX signal is being transmitted
  - L: Selected when the FAX signal is being received

8. CI detection circuit

The CI detection circuit detects the CI signals of 15.3 Hz to 68 Hz. A CI signal, which is provided to the photo-coupler PC1 through the C15 (0.82 μF), R1 (22 K), R2 (13K) and ZD3 when the ring signal is inputted from the telephone line, is filtered by the R137 and C9 and then transmitted to the control PWB through the Q110 (DTC114).

9. Power supply and bias circuits

The voltages of +12V and +5V are supplied from the control PWB unit. The IC104 of operational amplifier generates 6V bias voltage and supplies it to the IC104, 106, 105.

(Example: Fax signal send)

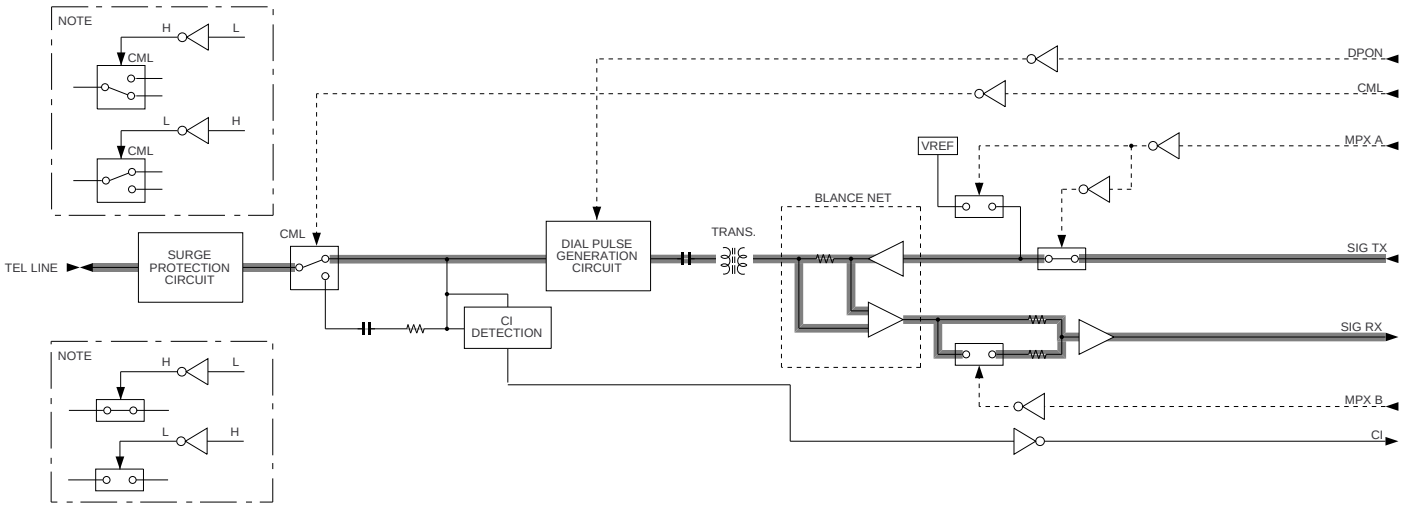


Fig. 11

Matrix table of control signals

		CML	MPXA	MPXB	MIC MUTE	RCV MUTE	SP MUTE
		H: ON L: OFF	H: TX LINE L: OFF	H: Low gain L: High gain	H: ON	H: ON	H: ON
Stand-by		L	L	L	H	H	H
FAX signal sending		H	H	H	H	H	H
FAX signal receiving		H	L	H	H	H	H
Auto dial	Before and after dialing	H	L	H	H	H	H
	300bps check	H	L	H	H	H	H
	DP dialing	L	L	H	H	H	H
	DTMF dialing	H	H	H	H	H	H

[6] Circuit description of CCD PWB

The CCD board picks up optical information from the document, converts it into an electrical (analog) signal and transfers it to the control board.

1. Block diagram

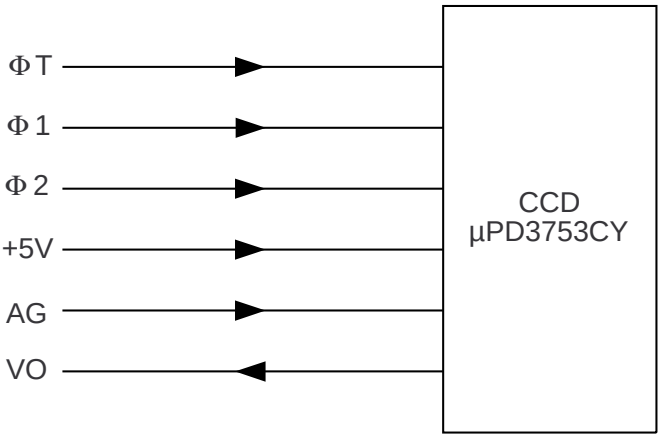


Fig.12

2. Description of blocks

1) CCD

The µPD3753CY is a highly sensitive charged coupled image sensor that consists of 2088 picture elements.
Receiving there drive signals (ϕT, ϕ2, ϕ1) from the control board.

2) Waveforms

1. ϕ1, ϕ2 ...signals within the control board.

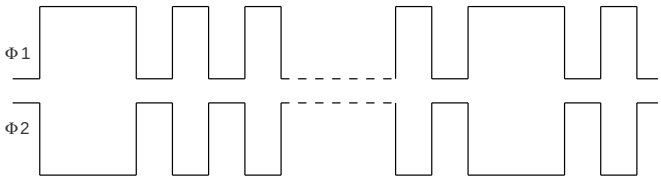


Fig. 13

[7] Circuit description of operation PWB

1. Block diagram

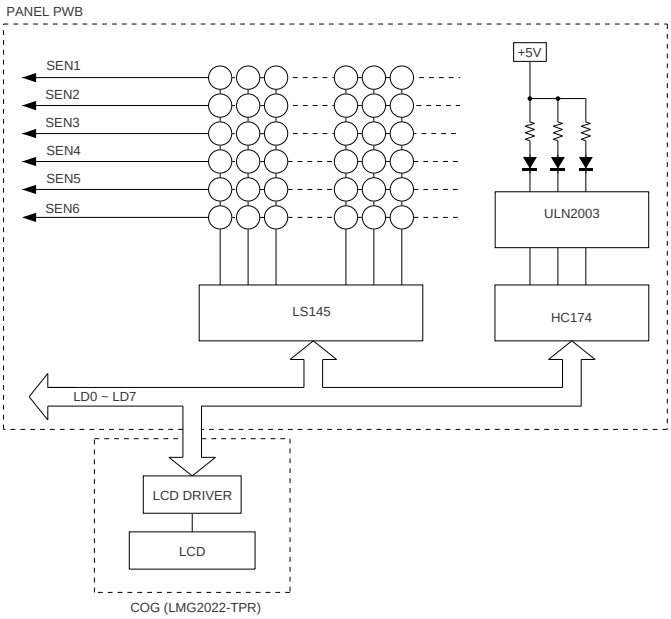


Fig. 14

2. Operational description

1) Panel PWB

The panel PWB includes the ten key scan circuit and the LED lighting circuit.The LS145 is controlled through LD0~LD3 (4 bits) and ten key detection is performed. The HC174 is controlled through LD0~LD5 (6 bits) to provide LED lighting information.

2) COG (LMG2022-TPR)

The COG uses the one-chip LCD driver IC to display 20 digits x 2 lines. The LCD display density is controlled with an extemal resistor.

[8] Circuit description of power supply PWB

DC power circuit

The DC power circuit directly rectifies AC power, changes the voltage through switching with the DC/DC converters, and rectifies and smoothens the current again in order to produce the DC voltage. See Fig. 15.

1. Block diagram

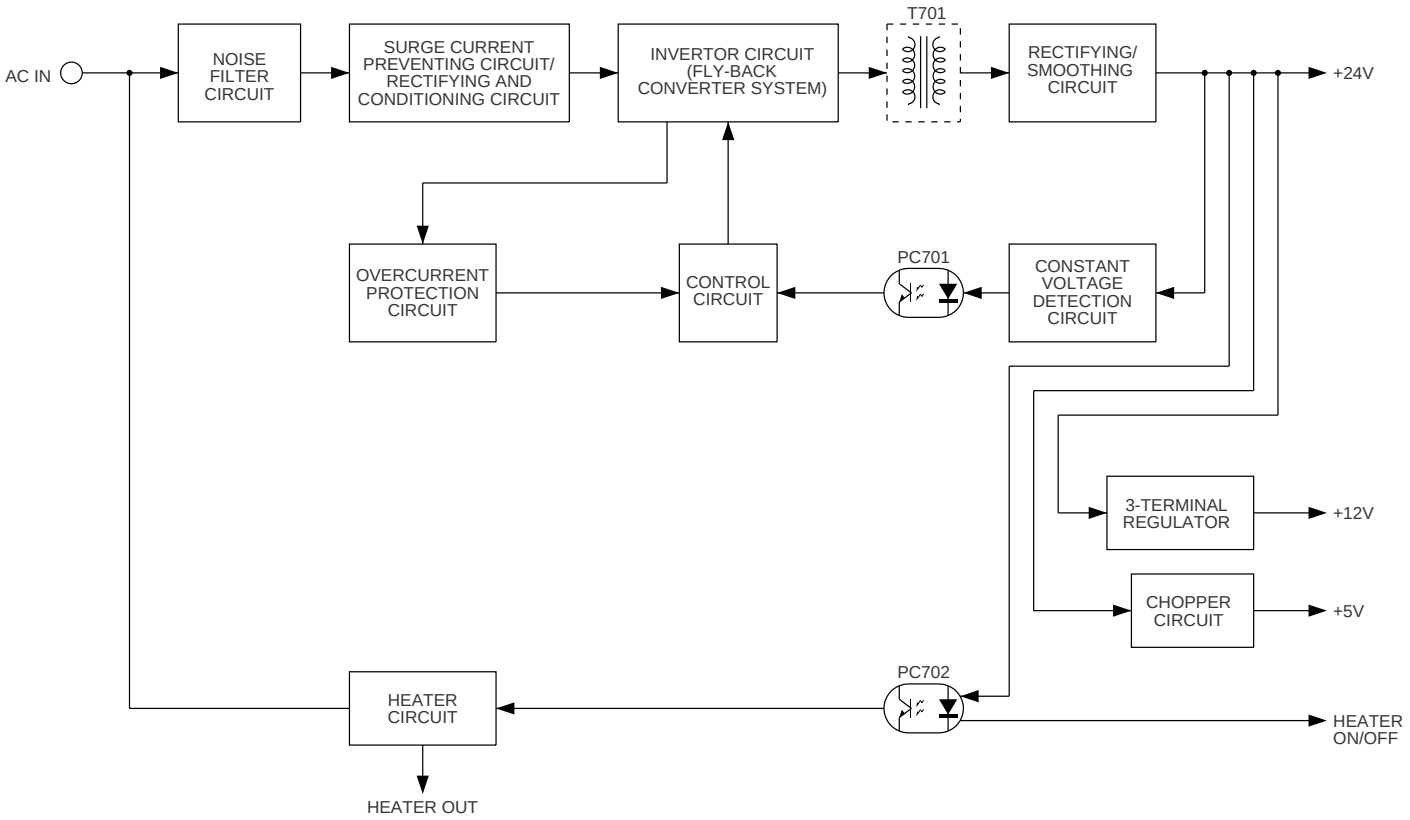


Fig. 15

2. Noise filter circuit

The filter circuit is composed of L and C in order to reduce the common noise and normal mode noise which flows into and out of the AC line.
The common mode noise is called the noise which generates in cach line against GND, and C703, C704, C722, C723 and C725 flows the noise component to GND.
Moreover, the normal mode noise is called the noise which is super-imposed on the AC line or output line and is attenuated with C701, L701, C702, and L702. See Fig. 16.

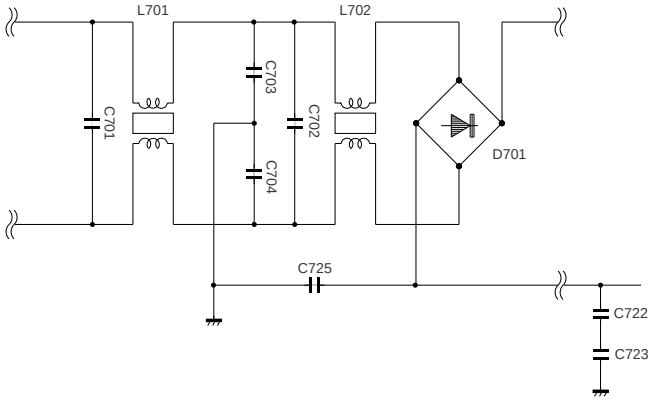


Fig. 16

3. Surge current preventing and rectifying/conditioning circuit

As shown in Fig. 17, AC is rectified and conditioned with D701 and C705 which include four diodes.
The power thermistor TH701 provide surge protection.

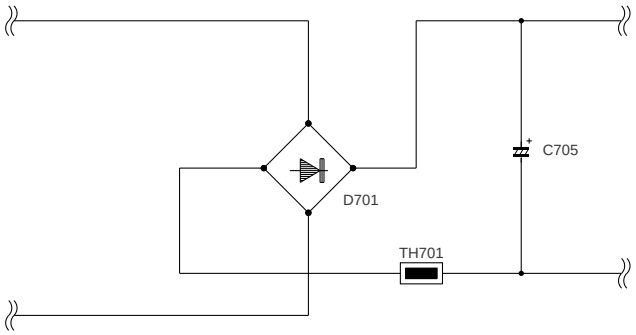


Fig. 17

4. Inverter and control circuit (fly-back converter system)

This circuit is called the fly-back converter which is the one-chip type separately excited DC-DC converter as shown in Fig. 18. In the circuit, IC starts oscillating to make Q701 conductive if the start voltage of IC is first applied to IC701 through R726, R794 and R705.
As the result, the voltage is applied to the primary winding of the converter transformer (T701), and the voltage is also generated in the winding which drives IC701. Thus IC701 is put into operation. Then, IC701 alternately turns on and off Q701 at the frequency (approx. 80 kHz) which is determined by C709 and R714.
When it is on, no current will flow in the secondary winding of T701 since the voltage of the secondary winding is applied in the direction opposite to the diode D707.
When it is off, the direction in which the current flows to the primary winding becomes the pole direction of the secondary winding, and D707 becomes conductive to transmit energy to the secondary side. See Fig. 18.

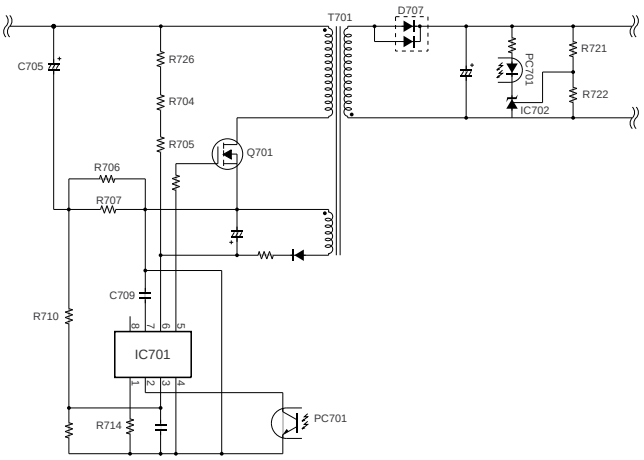


Fig. 18

The control circuit is a circuit which receives the negative feed-back is from the secondary side as shown in Fig. 18.
The photocoupler is used for insulation between the primary and secondary sides in order to feed back the control signal to the primary side. When the output voltage rises due to the energy transmission from T701, the voltage detected by R721 and R722 are compared with the reference voltage of IC702. As it is higher than the reference voltage, the current of IC702 (that is, the current of the photo diode of PC701) is increased to be transmitted to the primary side in order to reduce the potential of the feed-back terminal (2 pin) of IC701. Thus, Q701 is controlled. Accordingly, the varying rate of the output voltage on the primary side is passed through IC702 and PC701 in order to control IC701 and Q701. Thus, the output voltage is stabilized.

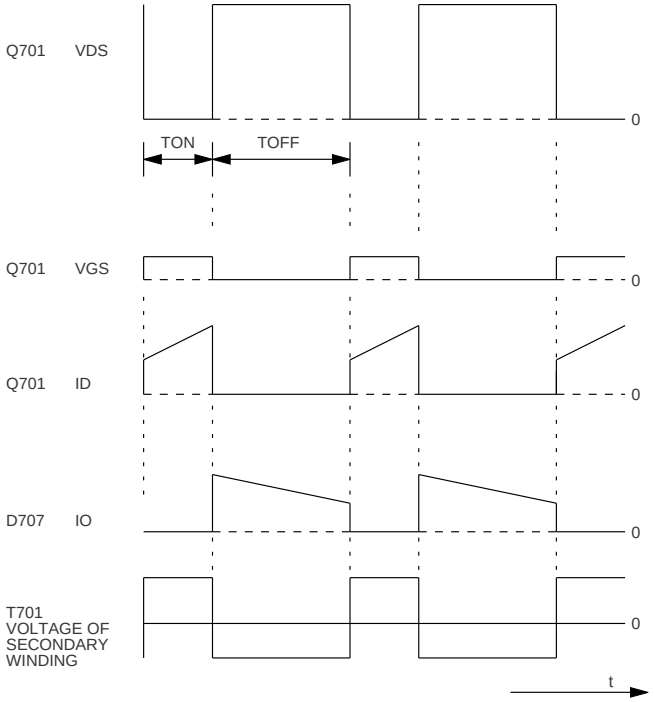


Fig. 19

IC701

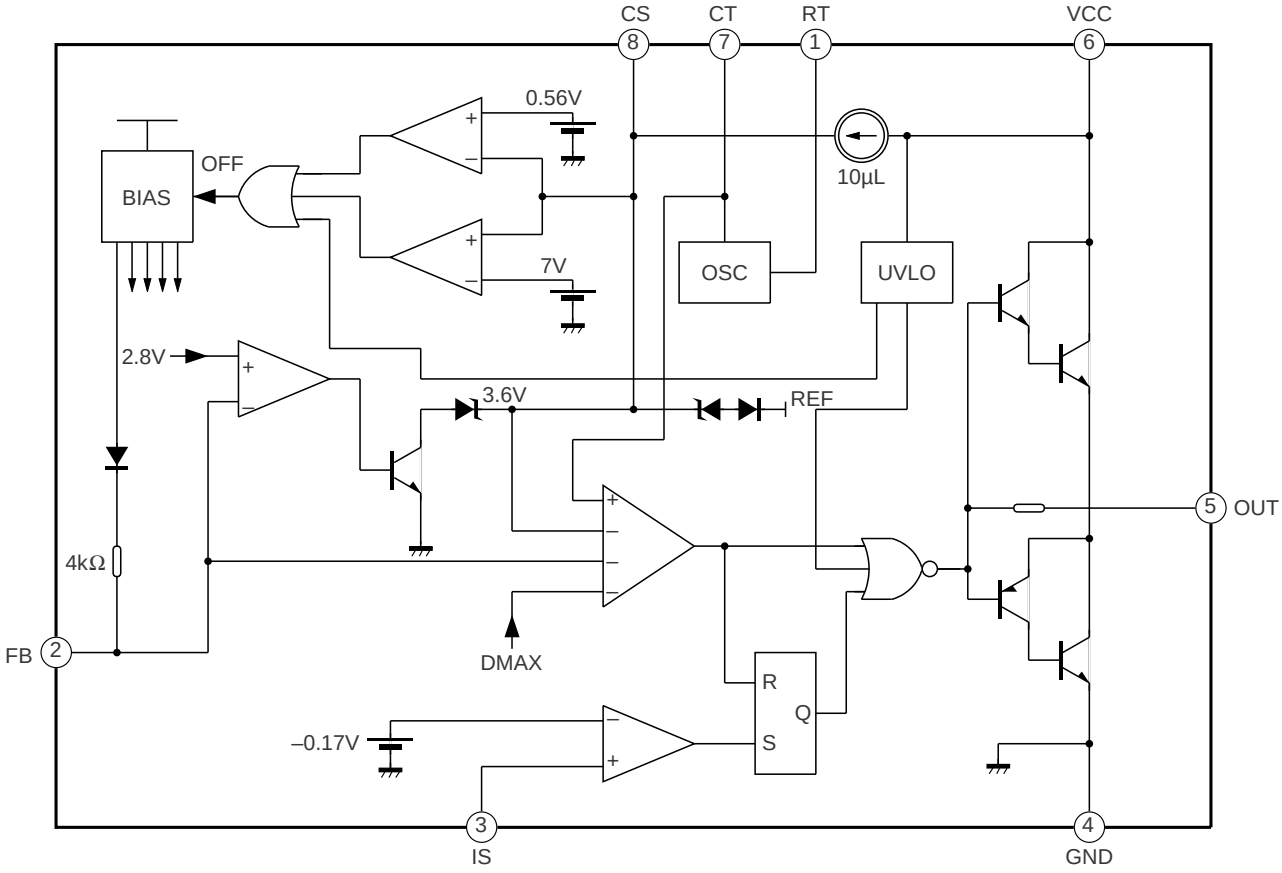


Fig. 20

5. Overcurrent preventive circuit (primary side)

The current detection resistors (R706 and R707) are connected to the inverter circuit on the primary side. If any overcurrent occurs on the primary side, the current of the inverter Q701 on the primary side is increased. The current is detected by R706 and R707, is passed through R710 and is input to the overcurrent restrictive terminal (3 pin) of IC701 to turn off Q701 in order to shut down the whole output. As the method to recover the power supply again, the power input is turned off again to sufficiently discharge the voltage of C705, and the power input is turned on (when 9V or less stands at the power terminal 6 pin of IC701).
A time of approx. 1 minute is necessary to discharge electricity from C705. See Fig. 18.

6. Rectifying/conditioning circuit (VM (+24V))

The high-frequency pulse produced in the inverter circuit is dropped by the converter transformer T701, is rectified by the high-frequency diode D707 and is moreover conditioned by C715 and 716.

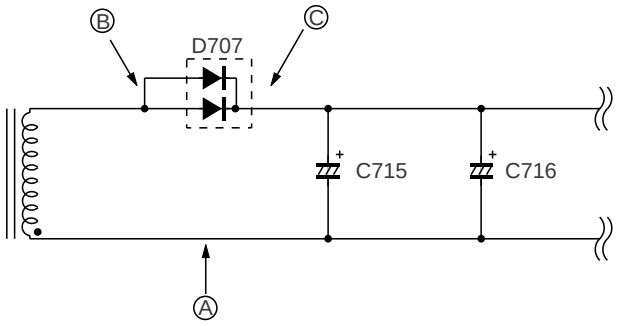


Fig. 21

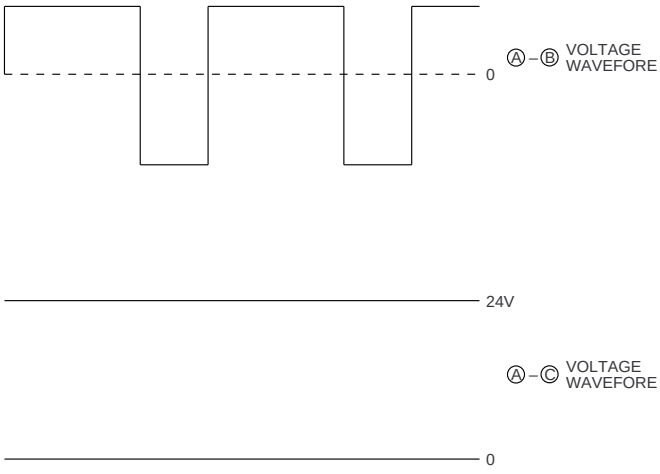


Fig. 22

7. 3-terminal regulator circuit (+12V system)

It is also called the dropper system. VM system (+24V) is dropped to +12V with IC704 for stabilization. Moreover, the overcurrent protective circuit is a IC integrated type with the characteristic of "#" letter.

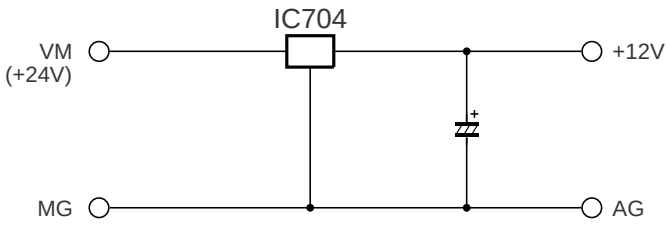


Fig. 23

8. Chopper circuit (+5V system)

The output voltage detected by R723 and R724 is input into the air amplifier by IC703, and is passed through the PWM comparator for PWA control of the output transistor in order to stabilize the output voltage. The oscillating frequency is set at approx. 100 kHz with the integrated oscillator. Moreover, the overcurrent-protective circuit is an IC integrated type to drop the output for the overcurrent.

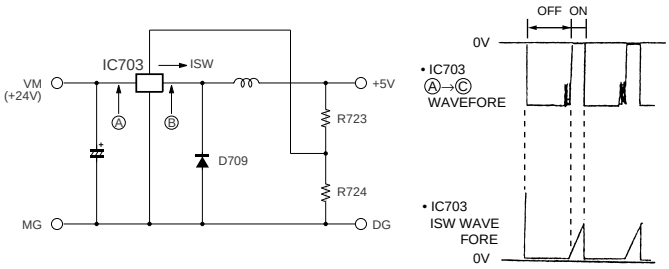


Fig. 24

IC703

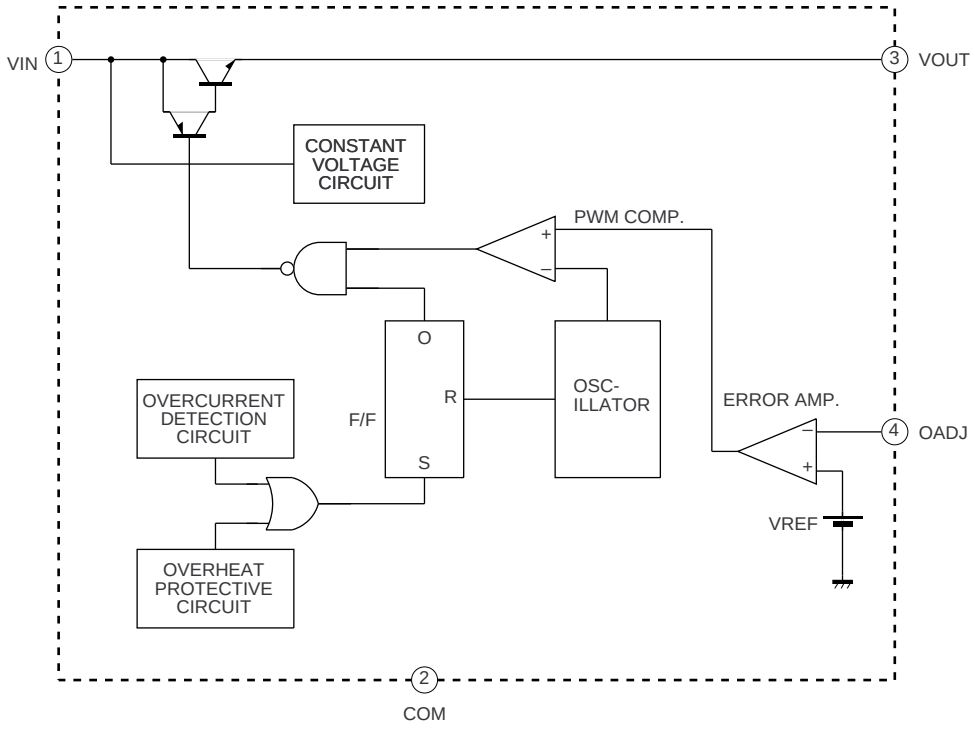


Fig. 25

9. Heater circuit

Though heater output is powered from AC line, the circuit is configured to allow one side of AC to be turned on and off by TR701.
When heater ON/OFF terminal is turned to LOW, the current will flow to the photo diode of PC702 to trigger the photo triac on the primary side and also turn on TR701.
This will activate the heater output. On the contrary, when the heater ON/OFF terminal is turned to HIGH, any current will not flow to the photo diode of PC702 to turn off TR701.
This will deactivate the heater output.
If TR701 is broken in the short mode, any current will not flow to the photo diode side of PC703 to turn off the photo transistor on the secondary side, and Q703 will not be turned off.
Q703 is connected to the gate cathode of SR701, and SR701 is usually turned off. However, when Q703 is turned off and the heater ON/OFF control terminal is further turned to HIGH, SR701 will be brought into the conductive state to cutoff the power supply to the heater circuit on the primary side.

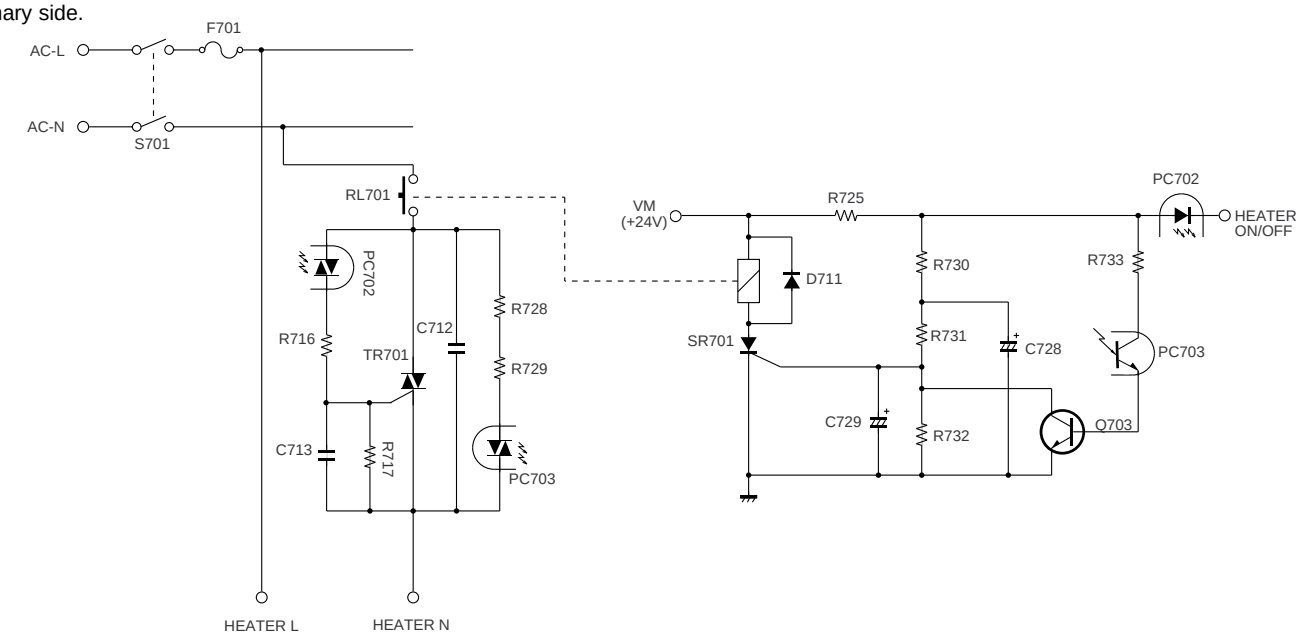


Fig. 26

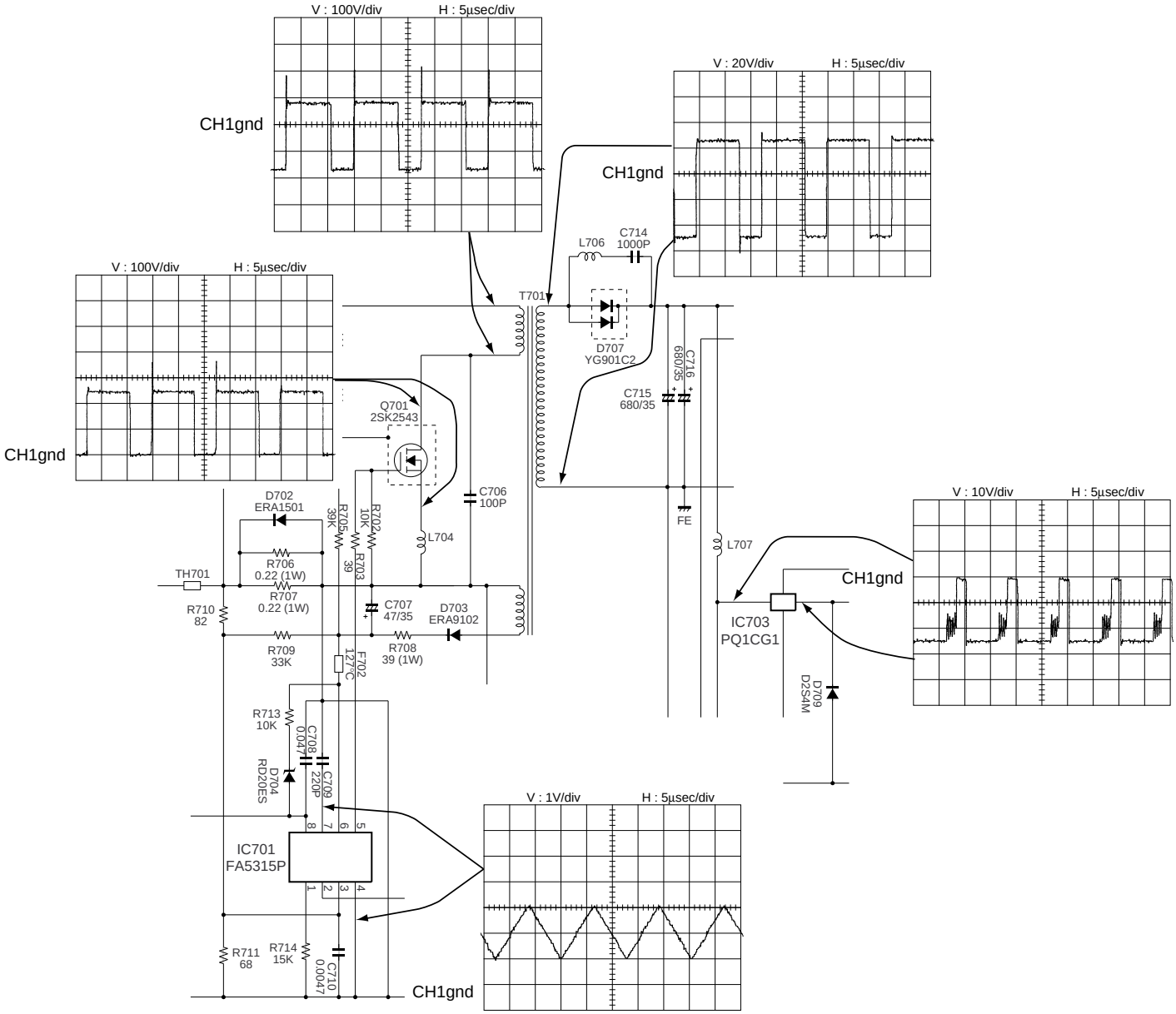


Fig. 27

[9] Circuit description of RS232C I/F PWB

Since the PWB uses RS232C as the interface with PC, the voltage of the signal from PC to the control PWB is converted to +5V level and the voltage of the signal from the control PWB to PC is converted to +12V level with IC1 (ADM207) on the PWB.